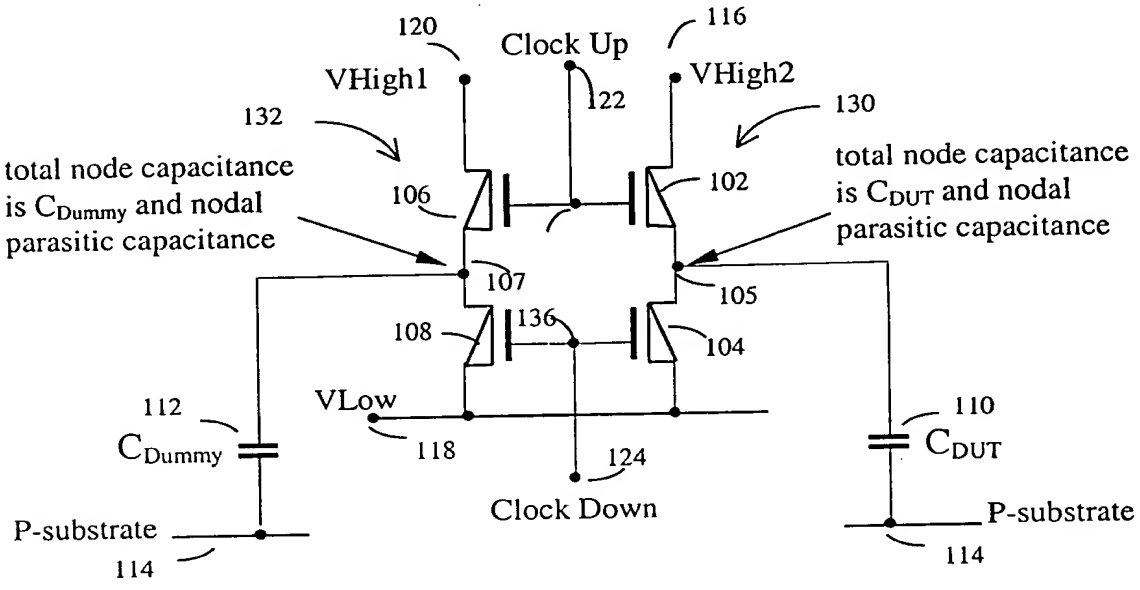
FIG.1


120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
107
105
108
136
104
112
VLow
110
C_{Dummy}
118
124
C_{DUT}
Clock Down
P-substrate
P-substrate
114
114

100

FIG. 2

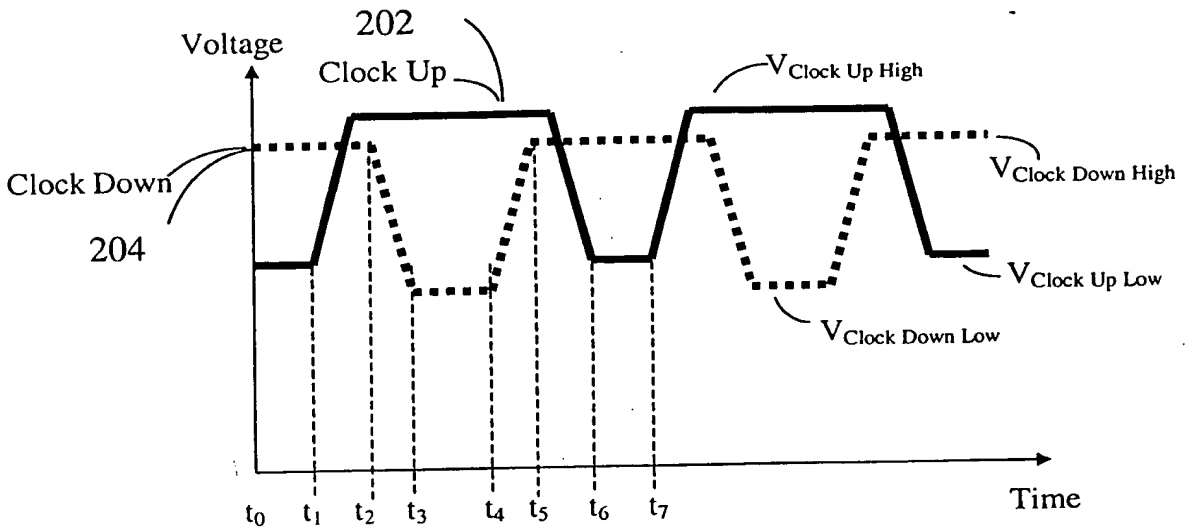

202
Voltage
Clock Up
$V_{Clock\ Up\ High}$
Clock Down
204
$V_{Clock\ Down\ High}$
$V_{Clock\ Up\ Low}$
$V_{Clock\ Down\ Low}$
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7
Time

FIG.3

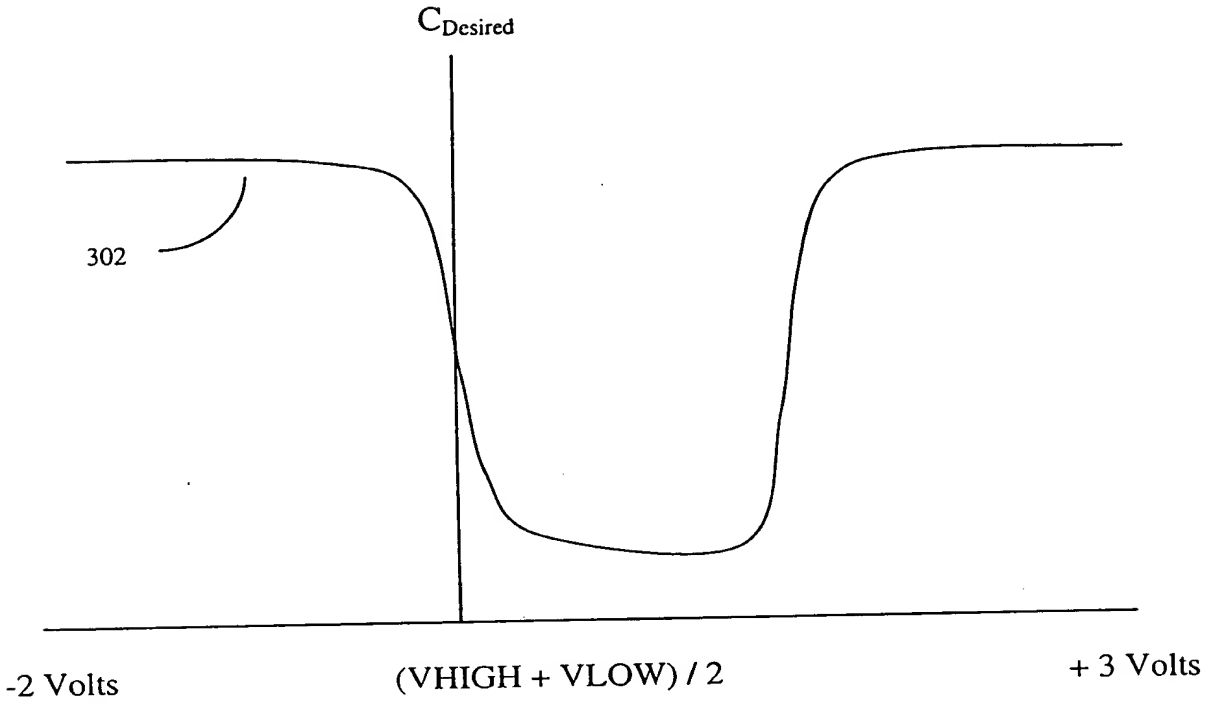


FIG. 4

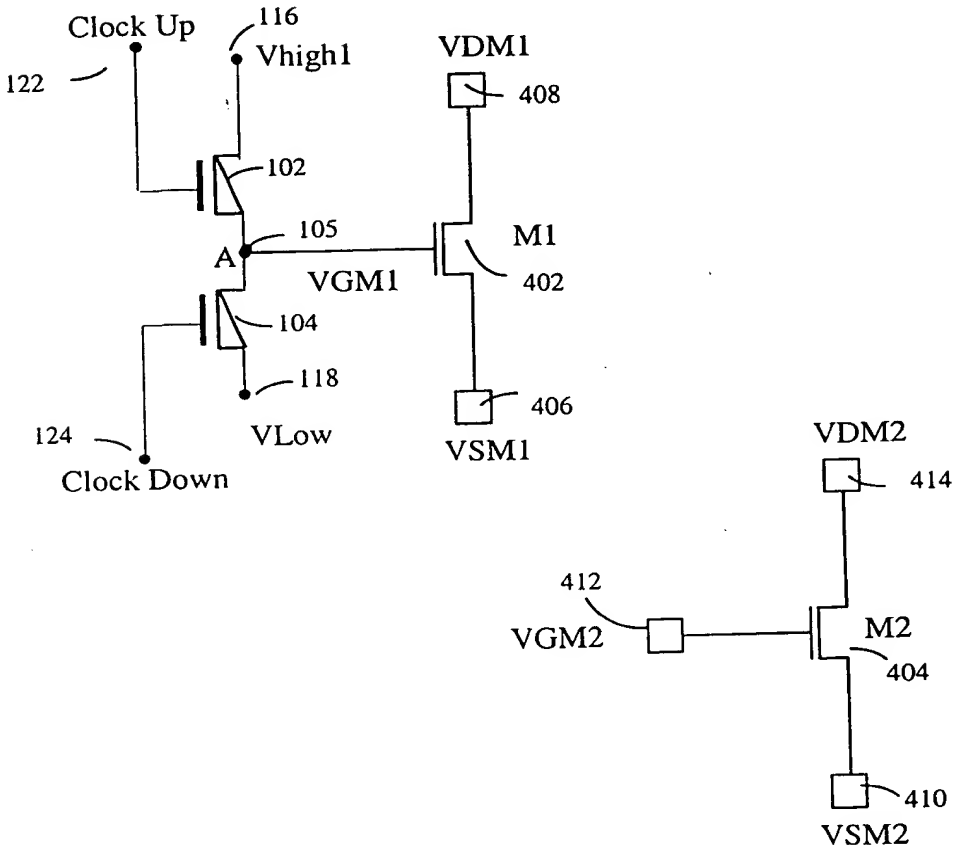
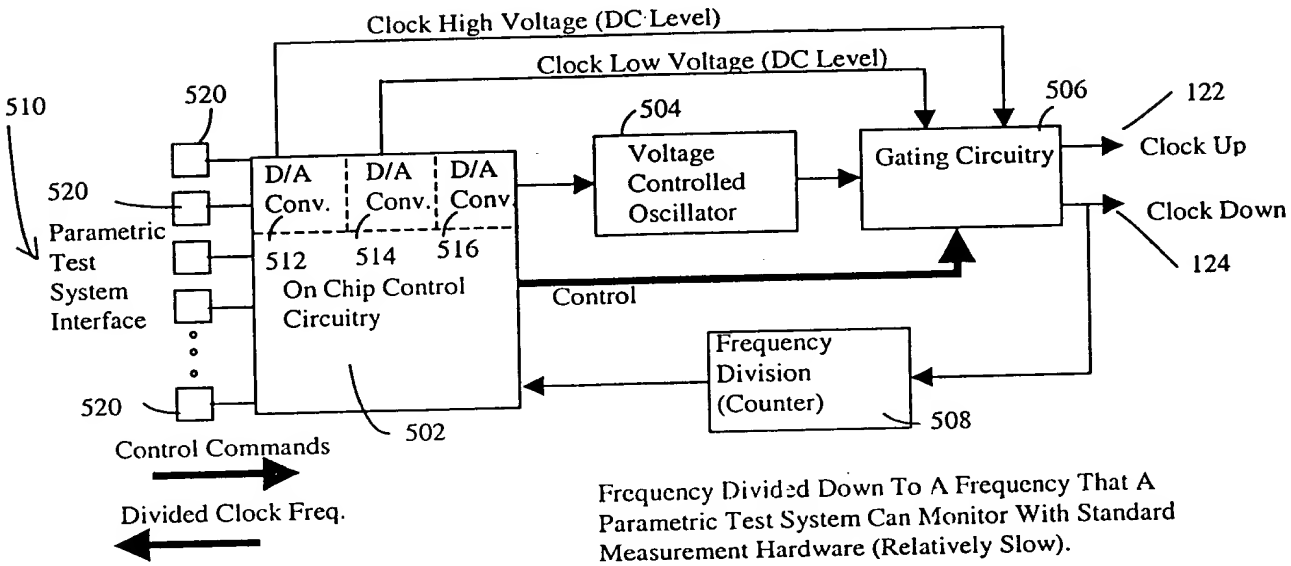
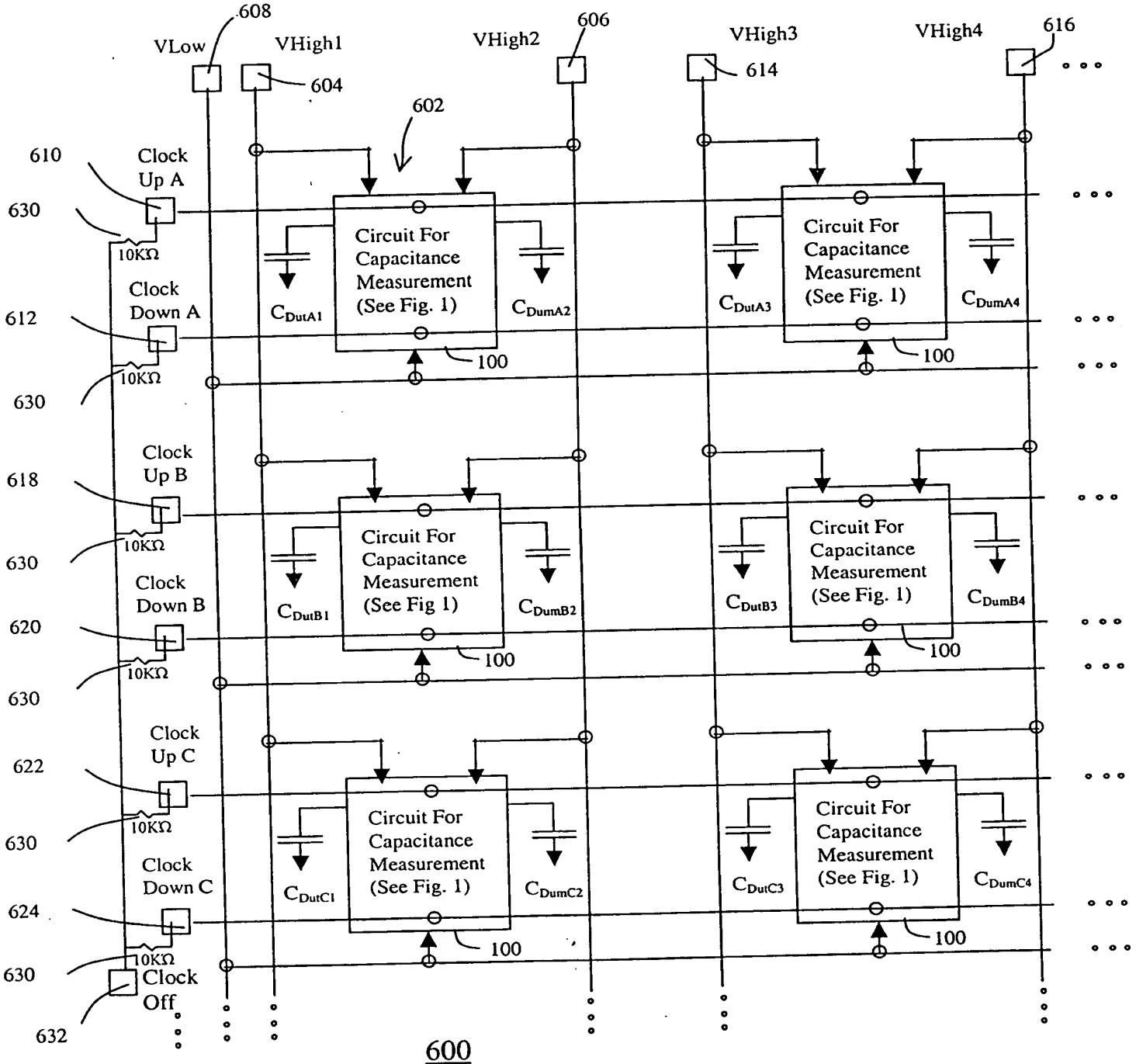

Clock Up
116
Vhigh1
VDM1
122
408
102
105
M1
A
VGM1
402
104
118
406
124
VLow
VSM1
Clock Down
VDM2
414
412
VGM2
M2
404
410
VSM2

FIG. 5


Clock High Voltage (DC Level)
Clock Low Voltage (DC Level)
510
520
520
Parametric Test System Interface
520
D/A Conv.
D/A Conv.
D/A Conv.
512
514
516
On Chip Control Circuitry
502
Control Commands
Divided Clock Freq.
504
Voltage Controlled Oscillator
506
Gating Circuitry
122
Clock Up
Clock Down
124
Control
Frequency Division (Counter)
508
Frequency Divided Down To A Frequency That A Parametric Test System Can Monitor With Standard Measurement Hardware (Relatively Slow).

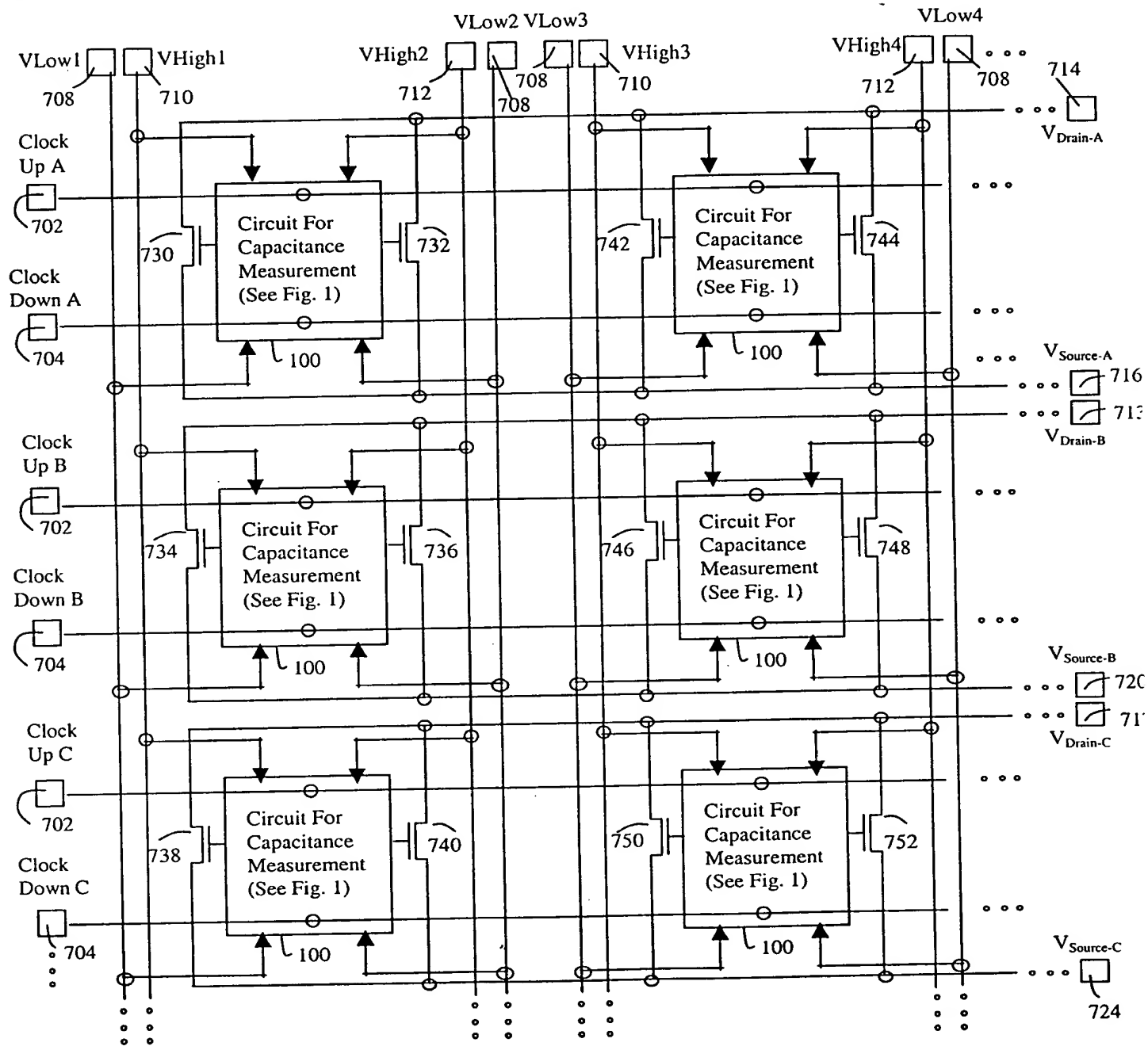
500

FIG. 6


608
606
616
VLow
VHigh1
VHigh2
VHigh3
VHigh4
604
614
602
610
Clock Up A
630
10KΩ
Clock Down A
612
630
618
Clock Up B
630
Clock Down B
620
630
622
Clock Up C
630
Clock Down C
624
630
Clock Off
632
Circuit For Capacitance Measurement (See Fig. 1)
Circuit For Capacitance Measurement (See Fig 1)
100
C_{DutA1}
C_{DumA2}
C_{DutA3}
C_{DumA4}
C_{DutB1}
C_{DumB2}
C_{DutB3}
C_{DumB4}
C_{DutC1}
C_{DumC2}
C_{DutC3}
C_{DumC4}

600

FIG. 7


VLow1
VHigh1
VLow2 VLow3
VHigh2
VHigh3
VLow4
VHigh4
708
710
712
714
Clock Up A
Clock Down A
Clock Up B
Clock Down B
Clock Up C
Clock Down C
702
704
Circuit For Capacitance Measurement (See Fig. 1)
730
732
734
736
738
740
742
744
746
748
750
752
100
$V_{Drain-A}$
$V_{Source-A}$
716
$V_{Drain-B}$
$V_{Source-B}$
720
$V_{Drain-C}$
$V_{Source-C}$
724

700

FIG. 8

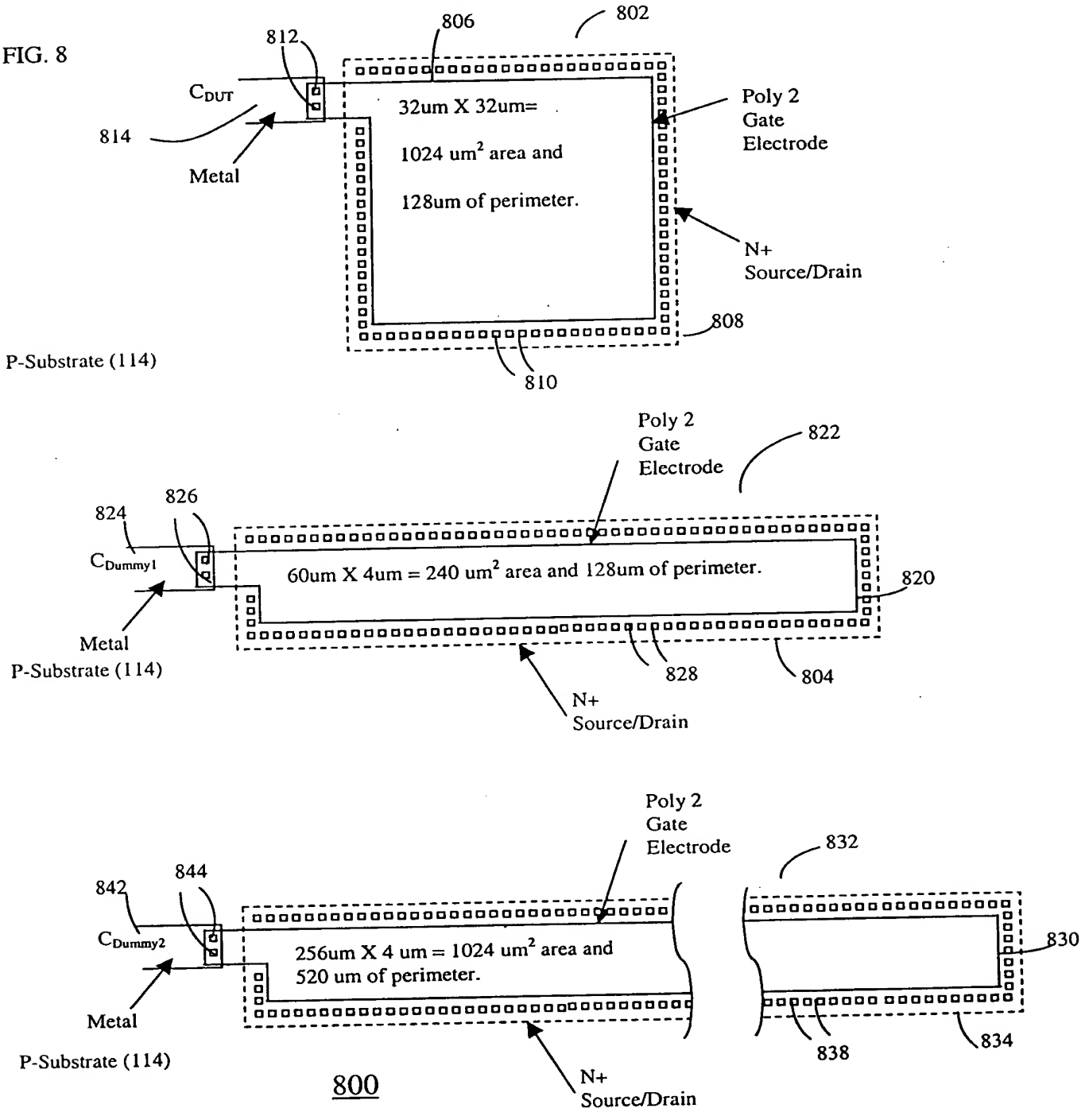

812
806
802
C_{DUT}
814
Metal
32um X 32um=
1024 um^2 area and
128um of perimeter.
Poly 2
Gate
Electrode
N+
Source/Drain
808
810
P-Substrate (114)
Poly 2
Gate
Electrode
822
826
824
C_{Dummy1}
60um X 4um = 240 um^2 area and 128um of perimeter.
820
Metal
P-Substrate (114)
828
804
N+
Source/Drain
Poly 2
Gate
Electrode
832
844
842
C_{Dummy2}
256um X 4 um = 1024 um^2 area and
520 um of perimeter.
830
Metal
838
834
P-Substrate (114)
N+
Source/Drain
800

FIG. 9

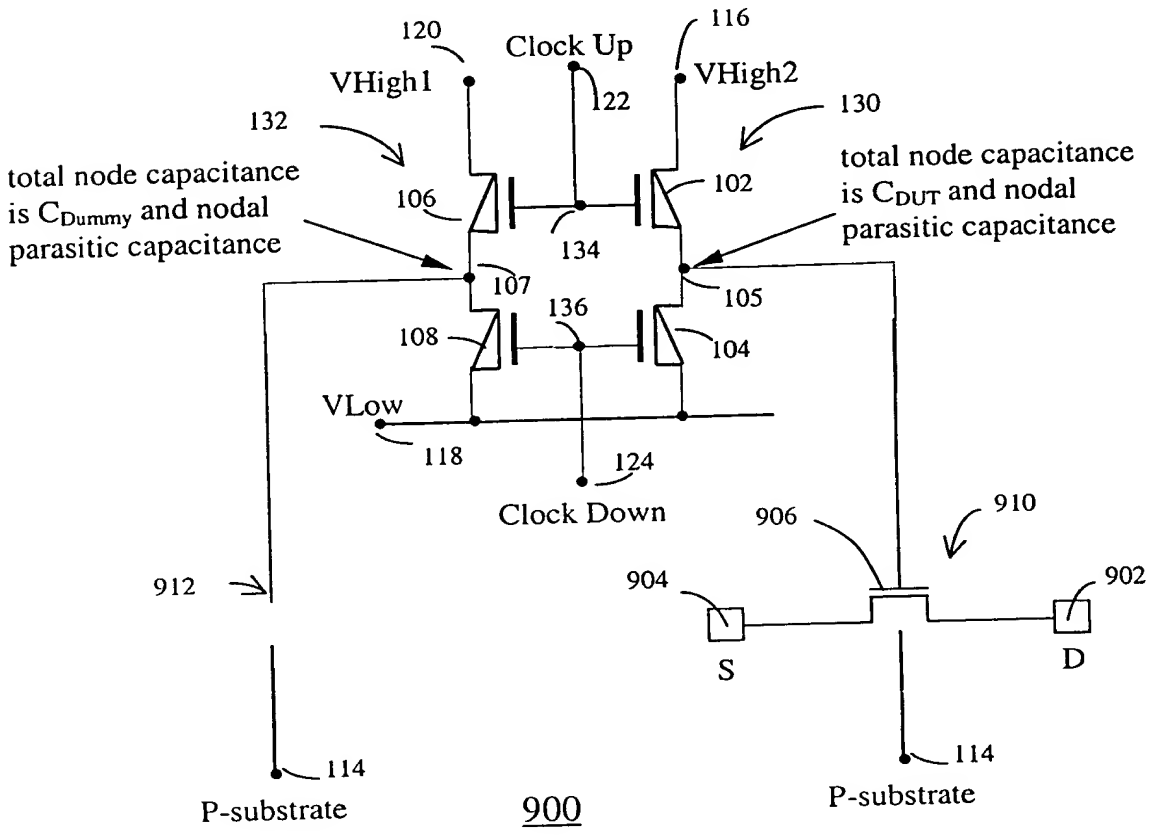

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
906
910
912
904
902
S
D
114
114
P-substrate
P-substrate
900

FIG. 10

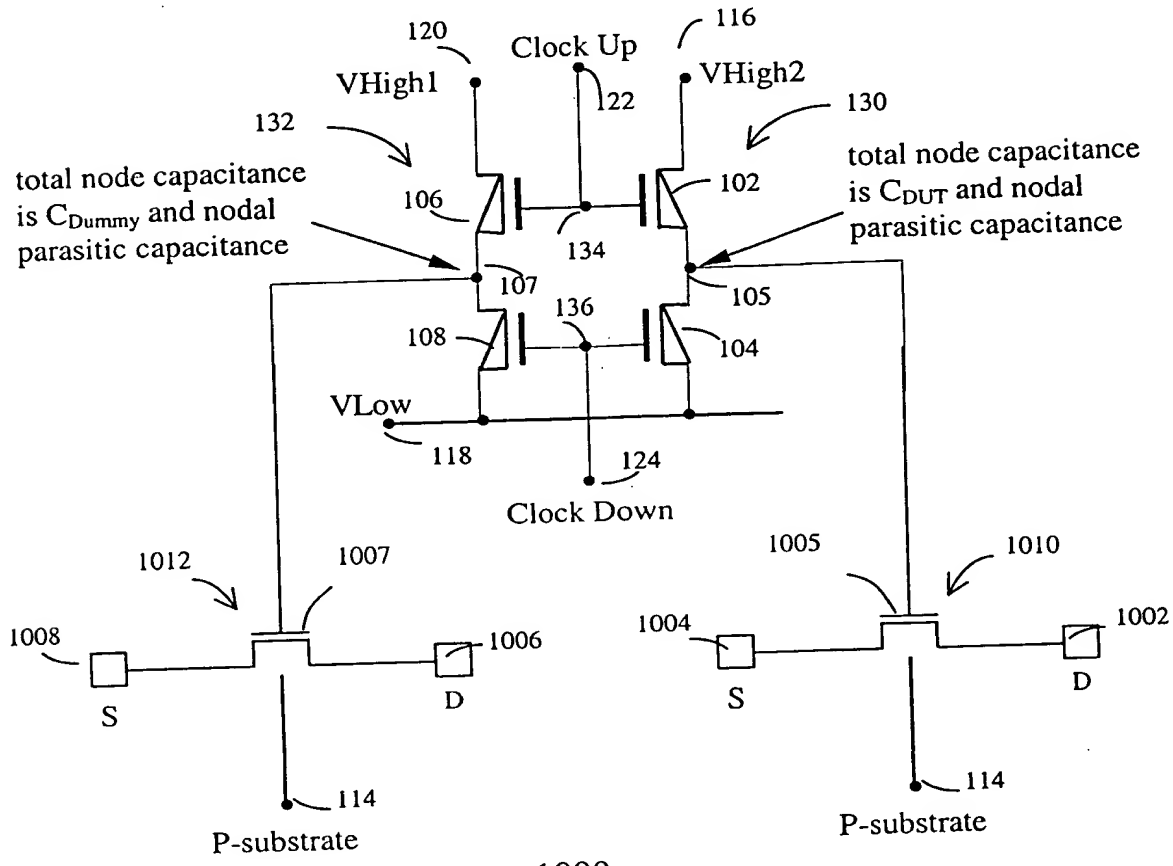

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1012
1007
1005
1010
1008
1006
1004
1002
S
D
S
D
114
114
P-substrate
P-substrate
1000

FIG. 11

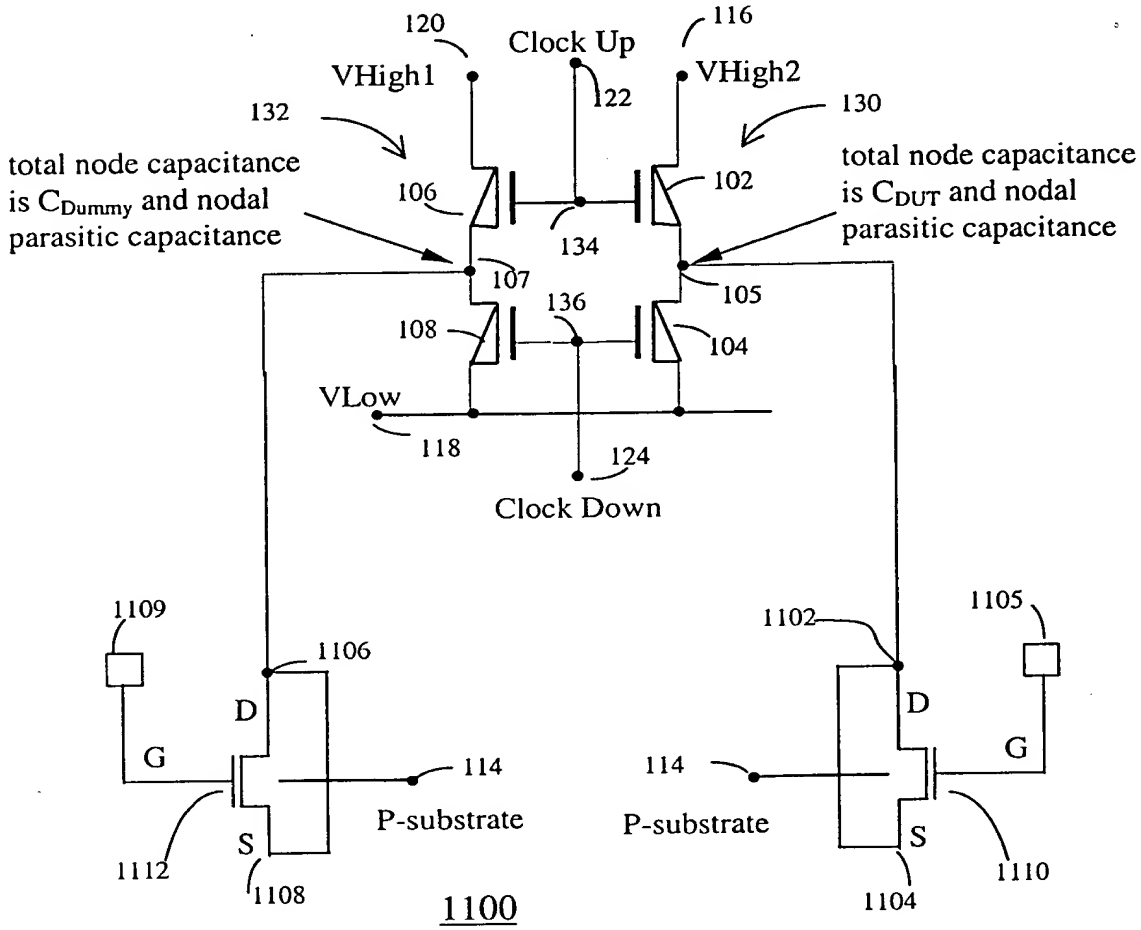

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1109
1106
1102
1105
D
D
G
G
114
114
P-substrate
P-substrate
S
S
1112
1108
1104
1110
1100

FIG. 12

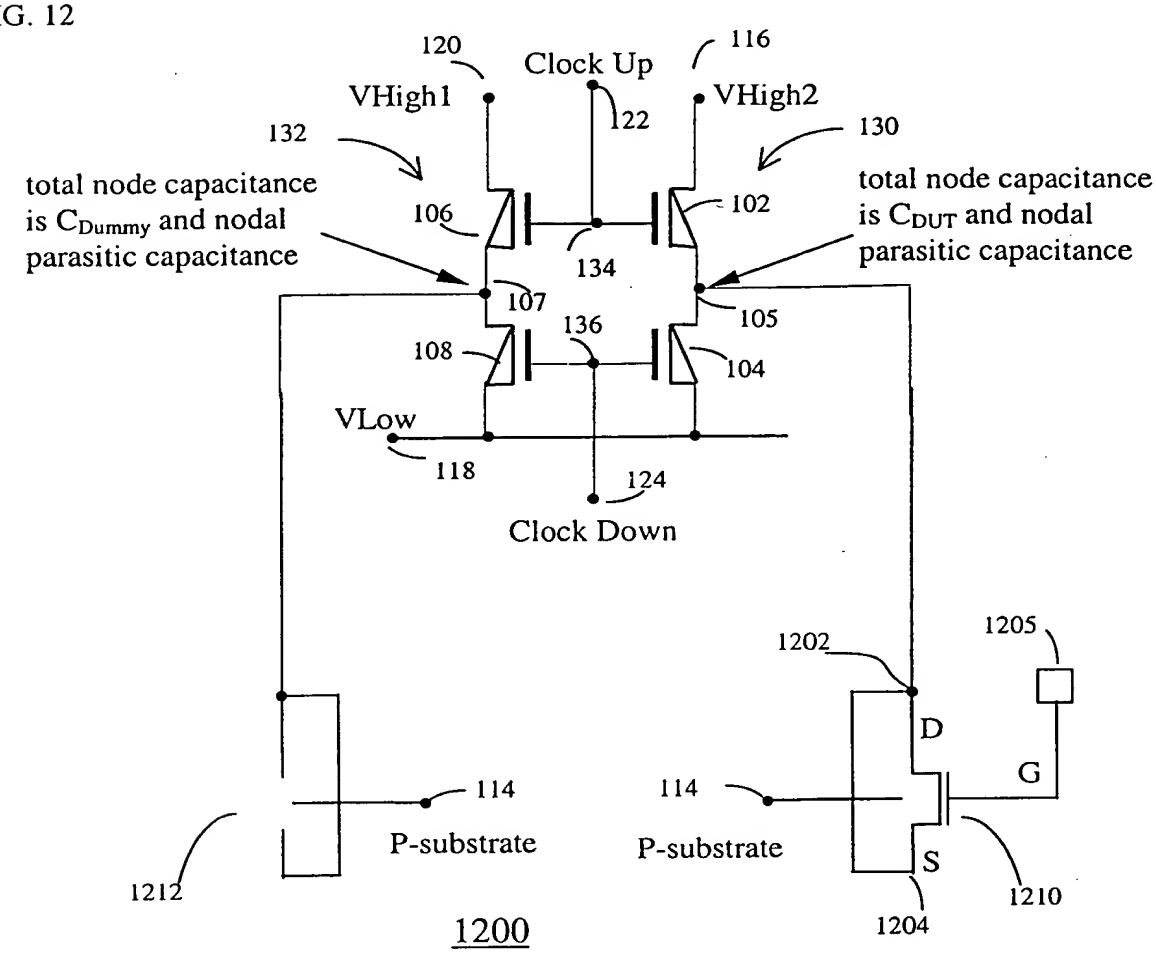

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1205
1202
D
G
114
114
P-substrate
P-substrate
S
1212
1210
1204
1200

FIG. 13

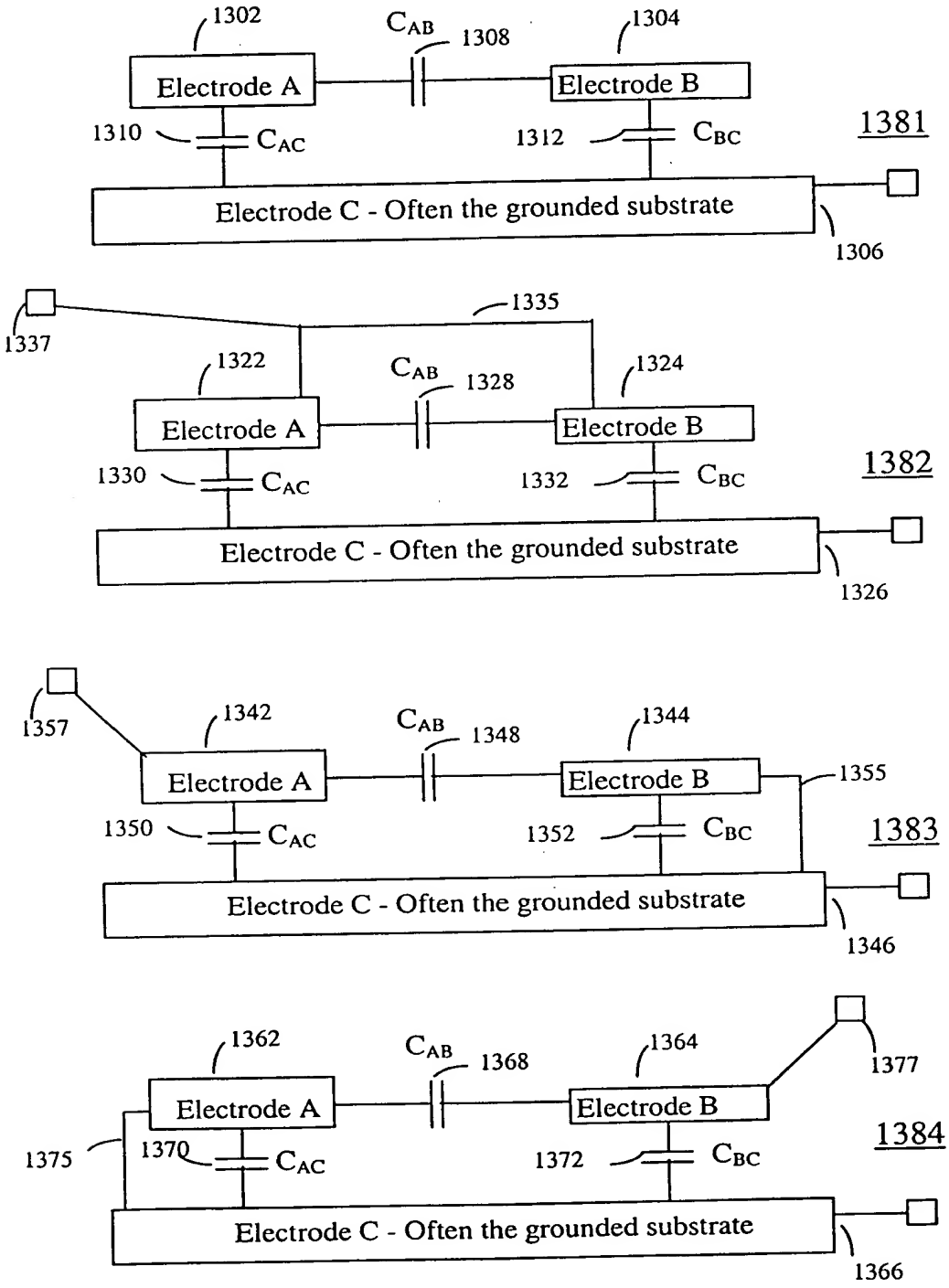

1302
C_{AB}
1308
1304
Electrode A
Electrode B
1310
C_{AC}
1312
C_{BC}
1381
Electrode C - Often the grounded substrate
1306
1337
1335
1322
C_{AB}
1328
1324
Electrode A
Electrode B
1330
C_{AC}
1332
C_{BC}
1382
Electrode C - Often the grounded substrate
1326
1357
1342
C_{AB}
1348
1344
Electrode A
Electrode B
1355
1350
C_{AC}
1352
C_{BC}
1383
Electrode C - Often the grounded substrate
1346
1362
C_{AB}
1368
1364
1377
Electrode A
Electrode B
1375
1370
C_{AC}
1372
C_{BC}
1384
Electrode C - Often the grounded substrate
1366

FIG. 14

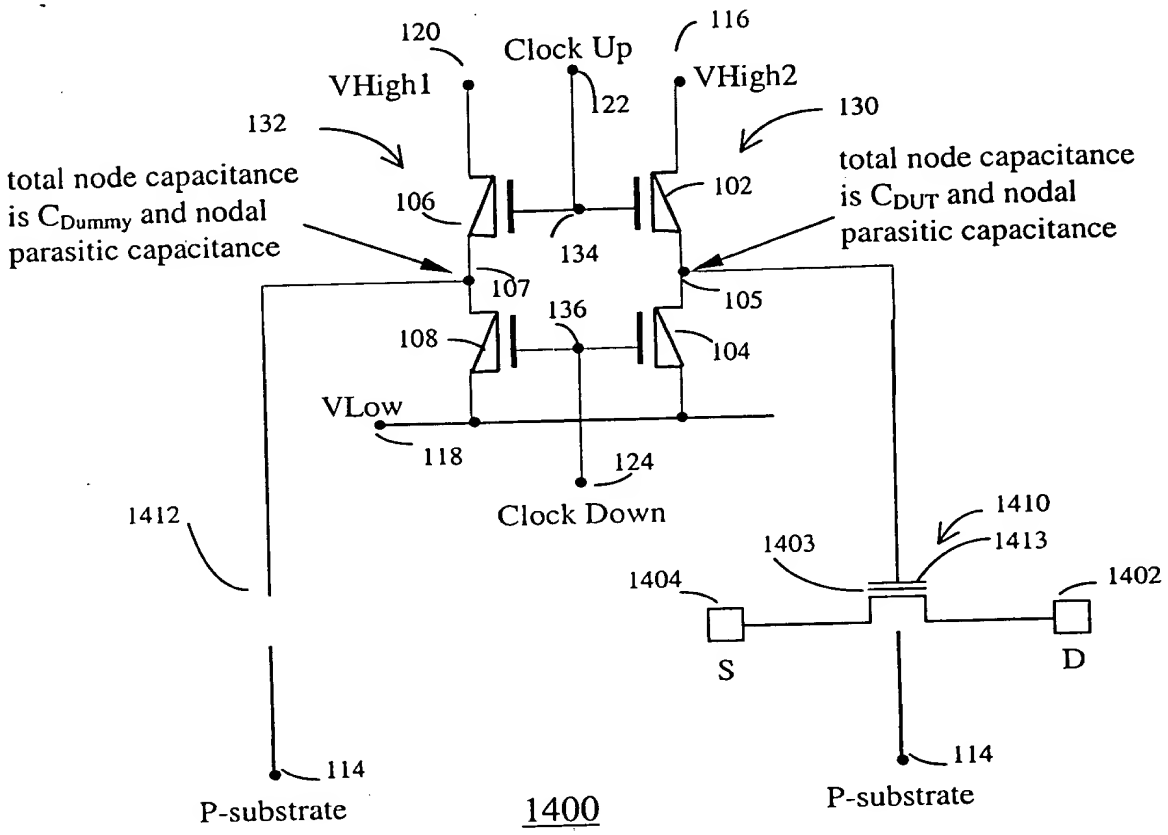

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1412
1410
1403
1413
1404
1402
S
D
114
114
P-substrate
P-substrate
1400

FIG. 15

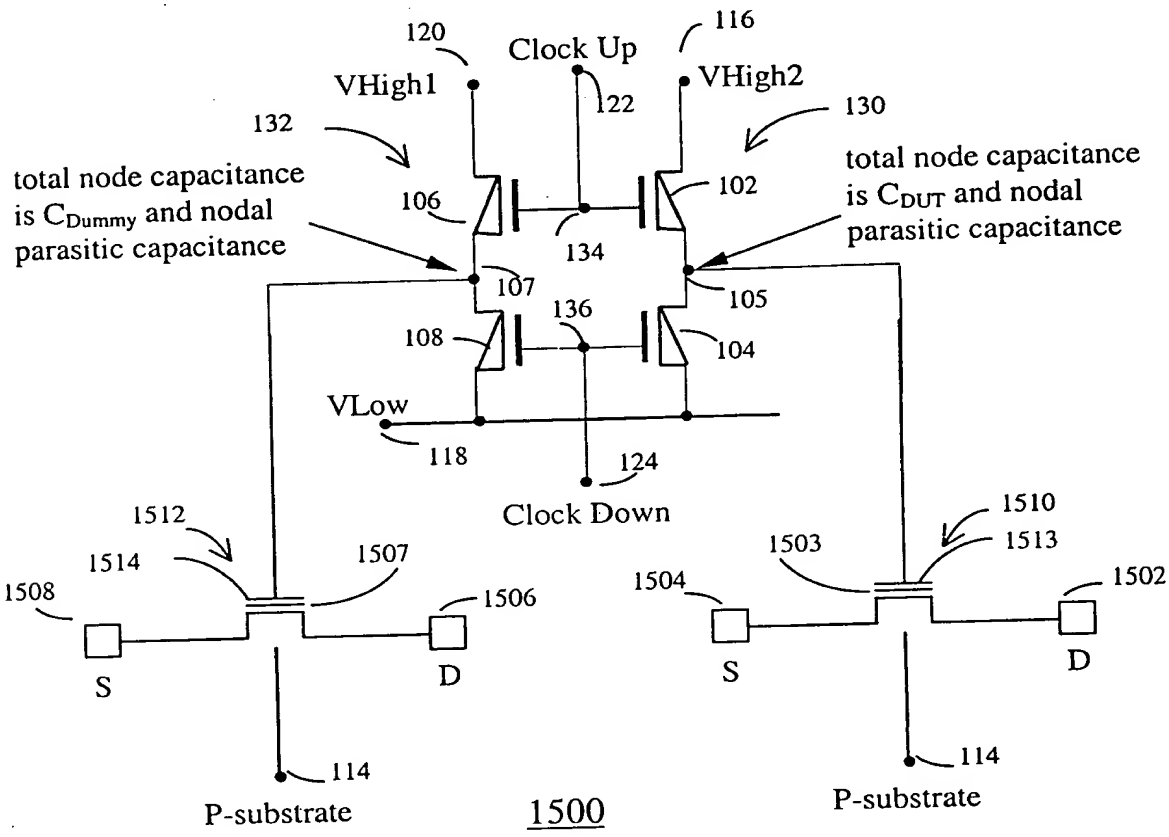

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1512
1514
1507
1510
1513
1503
1508
1506
1504
1502
S
D
S
D
114
114
P-substrate
P-substrate
1500

FIG. 16

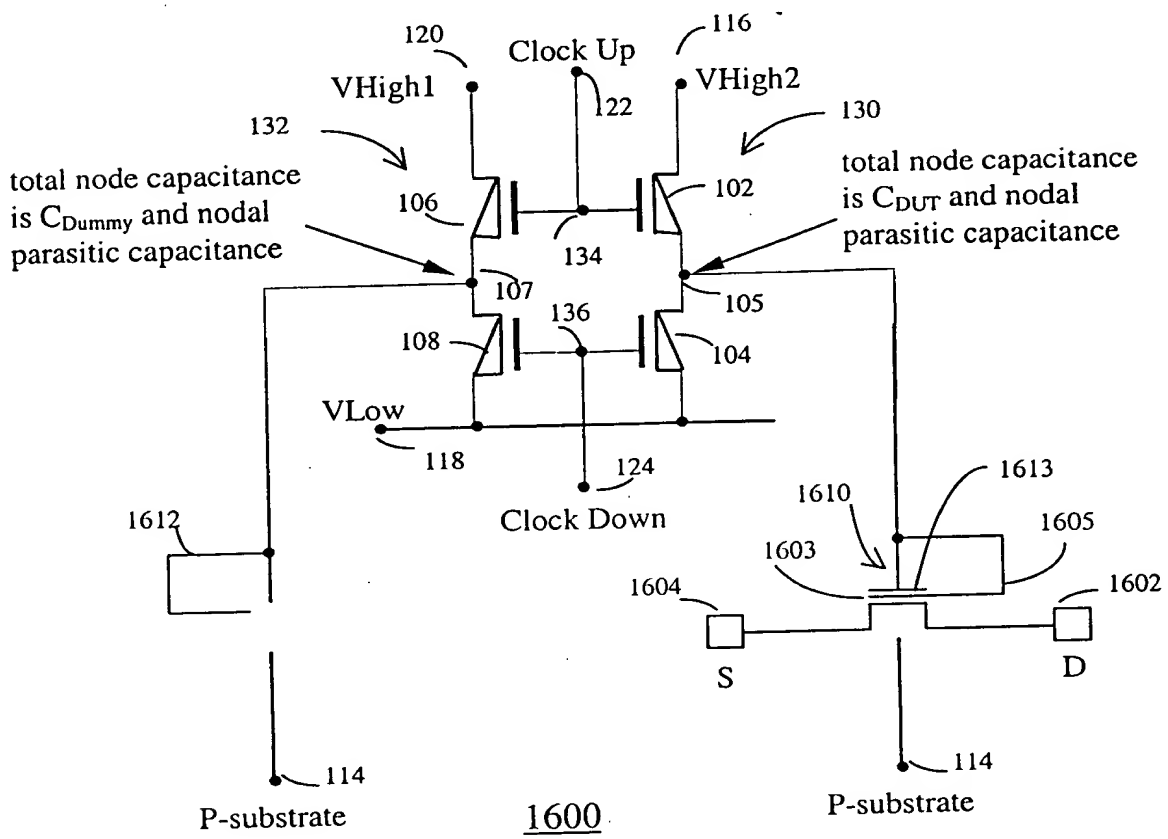

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1612
1610
1613
1605
1603
1604
1602
S
D
114
P-substrate
1600
114
P-substrate

FIG. 17

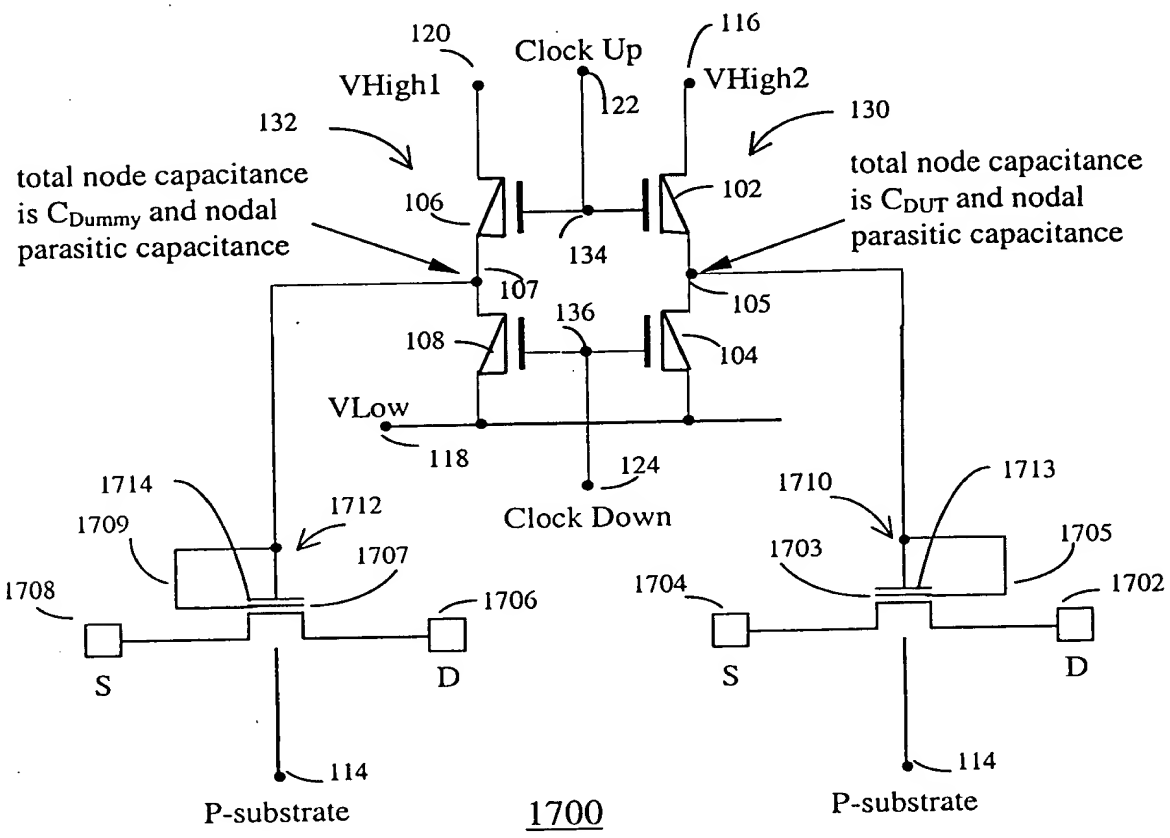

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1714
1712
1710
1713
1709
1707
1703
1705
1708
1706
1704
1702
S
D
S
D
114
114
P-substrate
P-substrate
1700

FIG. 18

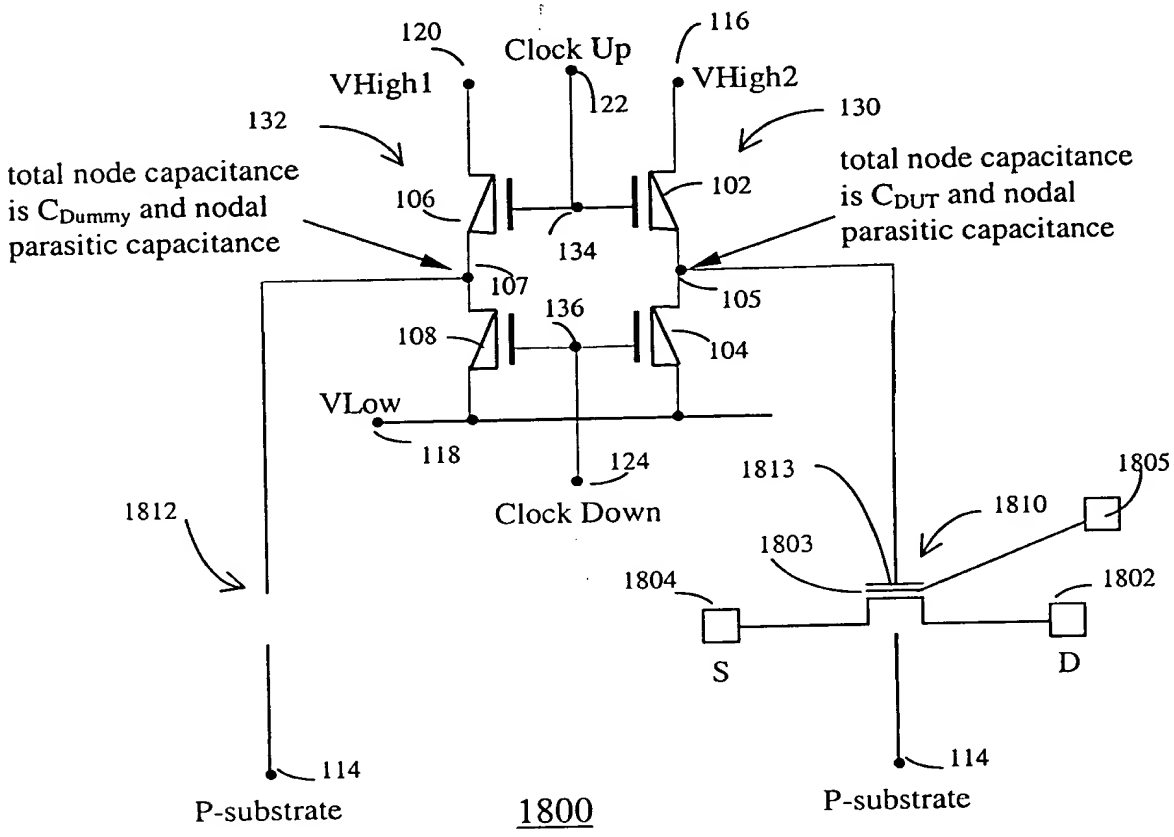

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1813
1805
1812
1810
1803
1804
1802
S
D
114
114
P-substrate
P-substrate
1800

FIG. 19

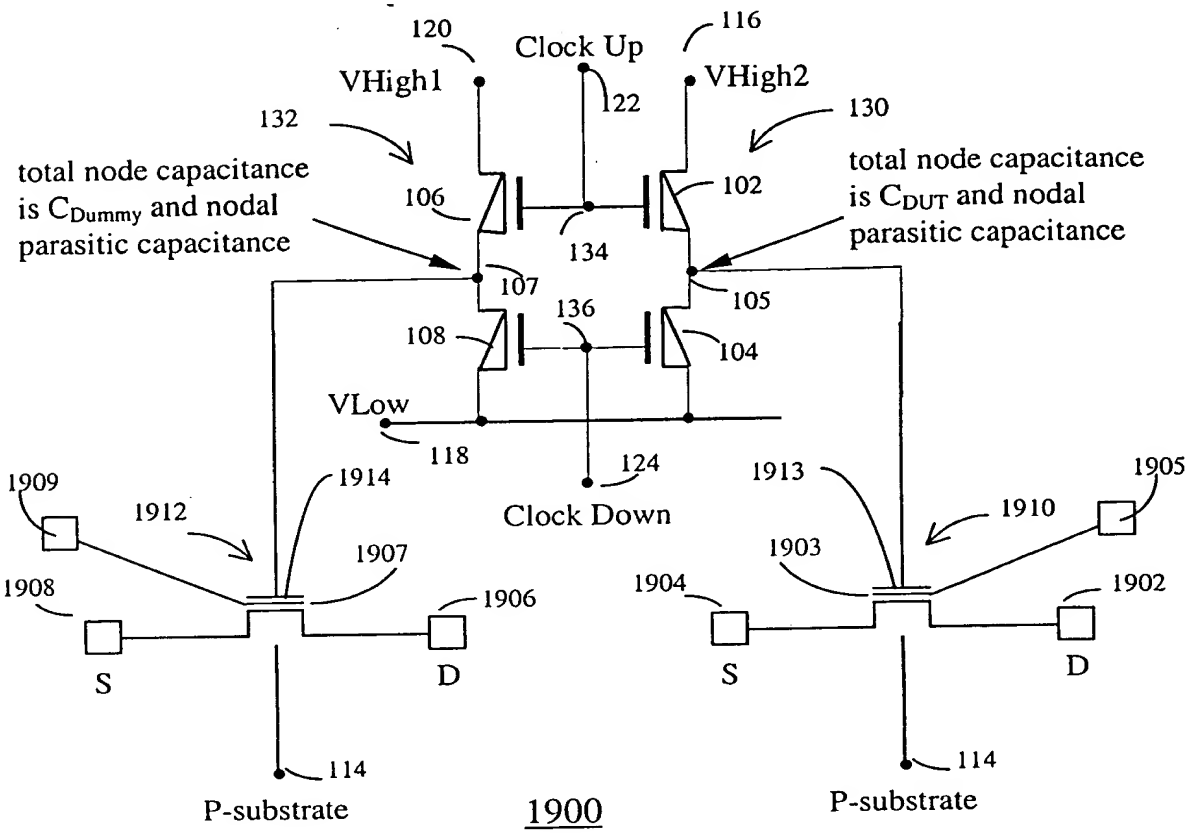

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
1909
1914
1913
1905
1912
1910
1907
1903
1908
1906
1904
1902
S
D
S
D
114
114
P-substrate
P-substrate
1900

FIG. 20

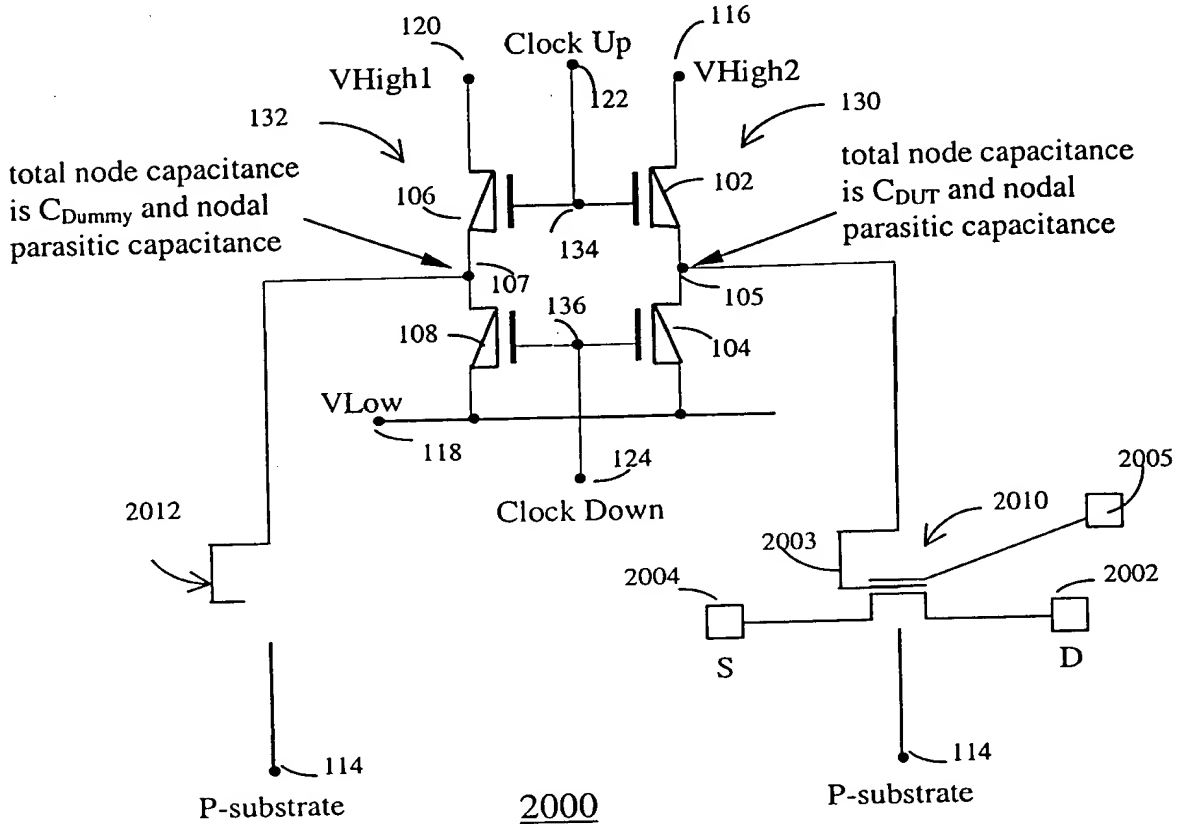

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
2005
2012
Clock Down
2010
2003
2004
2002
S
D
114
114
P-substrate
P-substrate
2000

FIG. 21

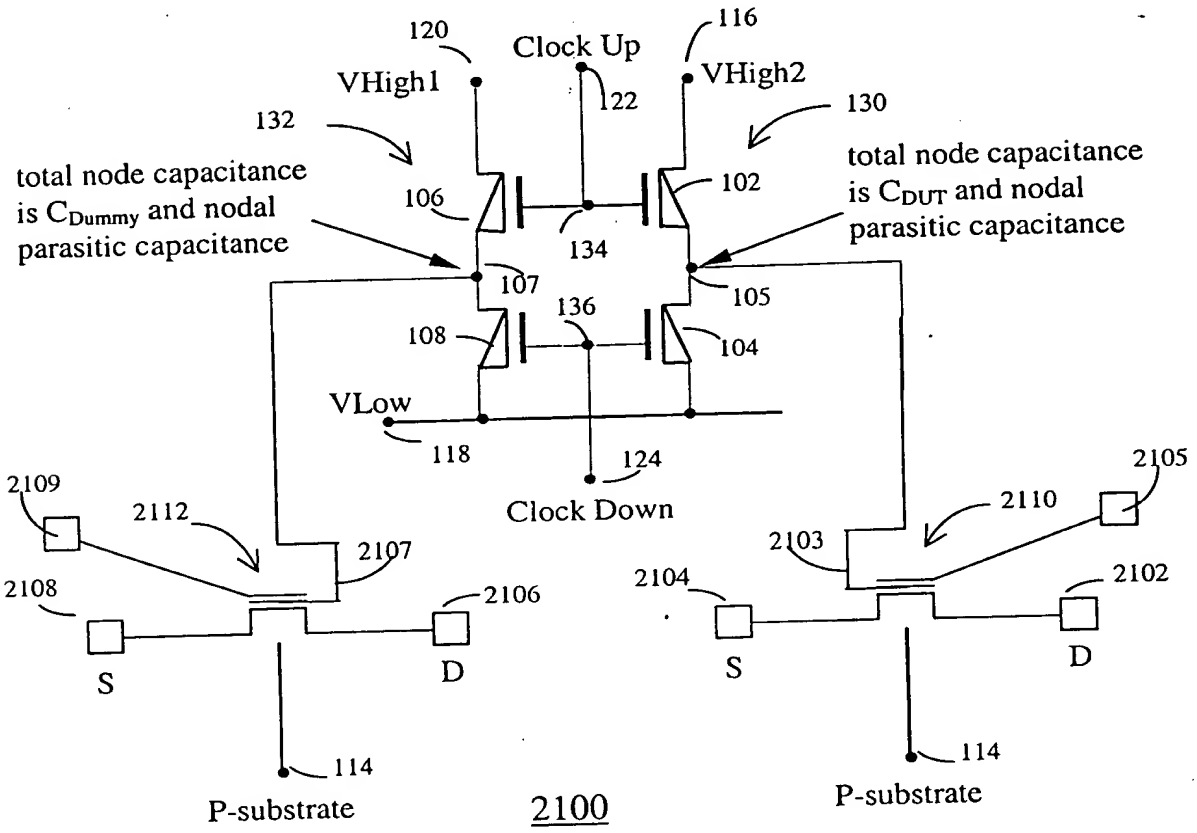
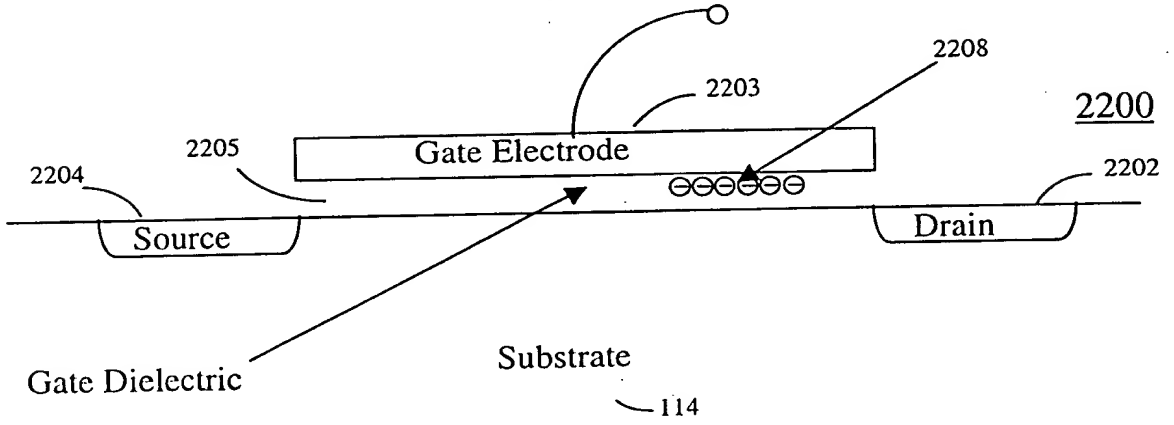
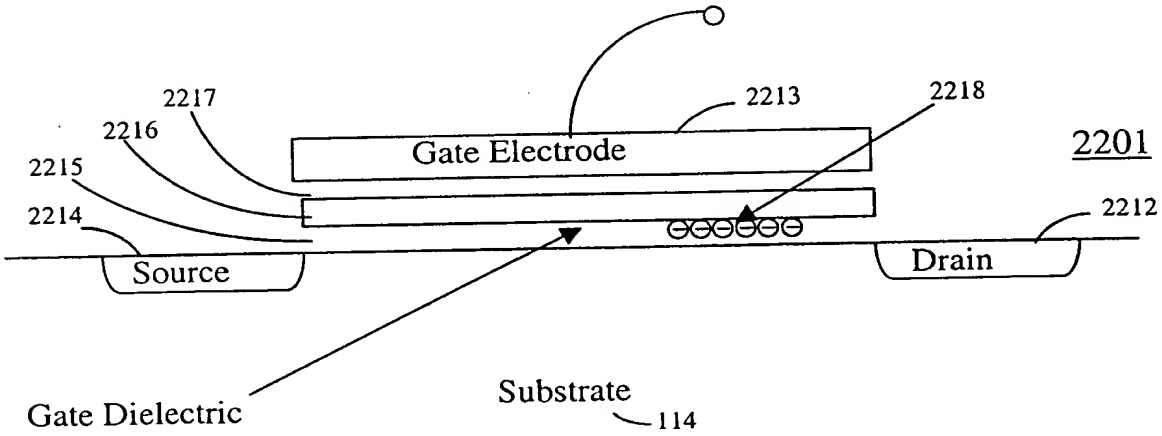

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
2109
2105
2112
2110
Clock Down
2107
2103
2108
2106
2104
2102
S
D
S
D
114
114
P-substrate
P-substrate
2100

FIG. 22


2208
2203
2200
Gate Electrode
2205
2204
2202
Source
Drain
Gate Dielectric
Substrate
114


2217
2213
2218
2216
Gate Electrode
2201
2215
2214
2212
Source
Drain
Gate Dielectric
Substrate
114

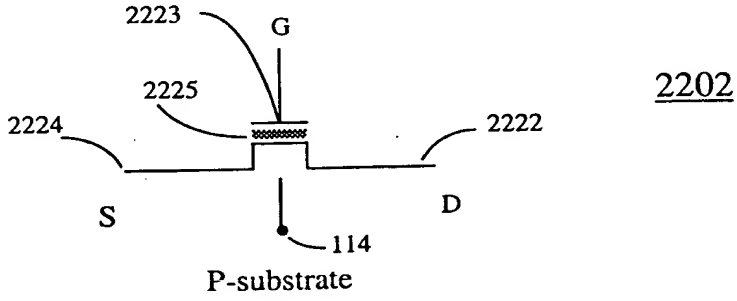

2223
G
2225
2202
2224
2222
S
D
114
P-substrate

FIG. 23:

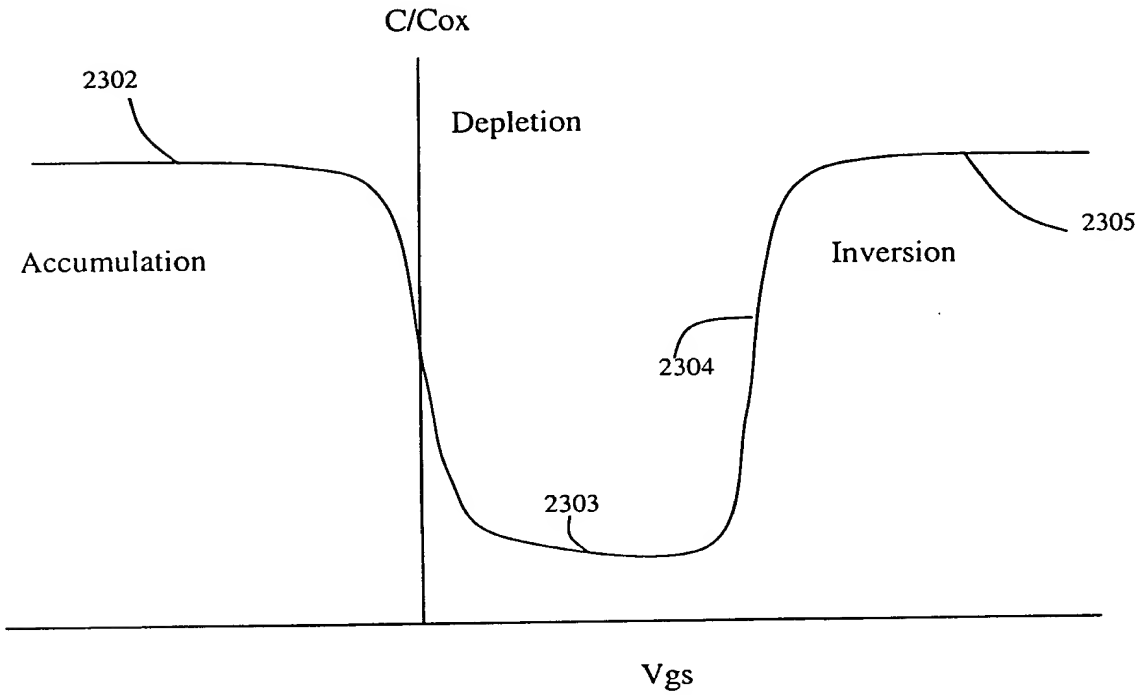

C/Cox
2302
Depletion
Accumulation
2305
Inversion
2304
2303
Vgs

FIG. 24

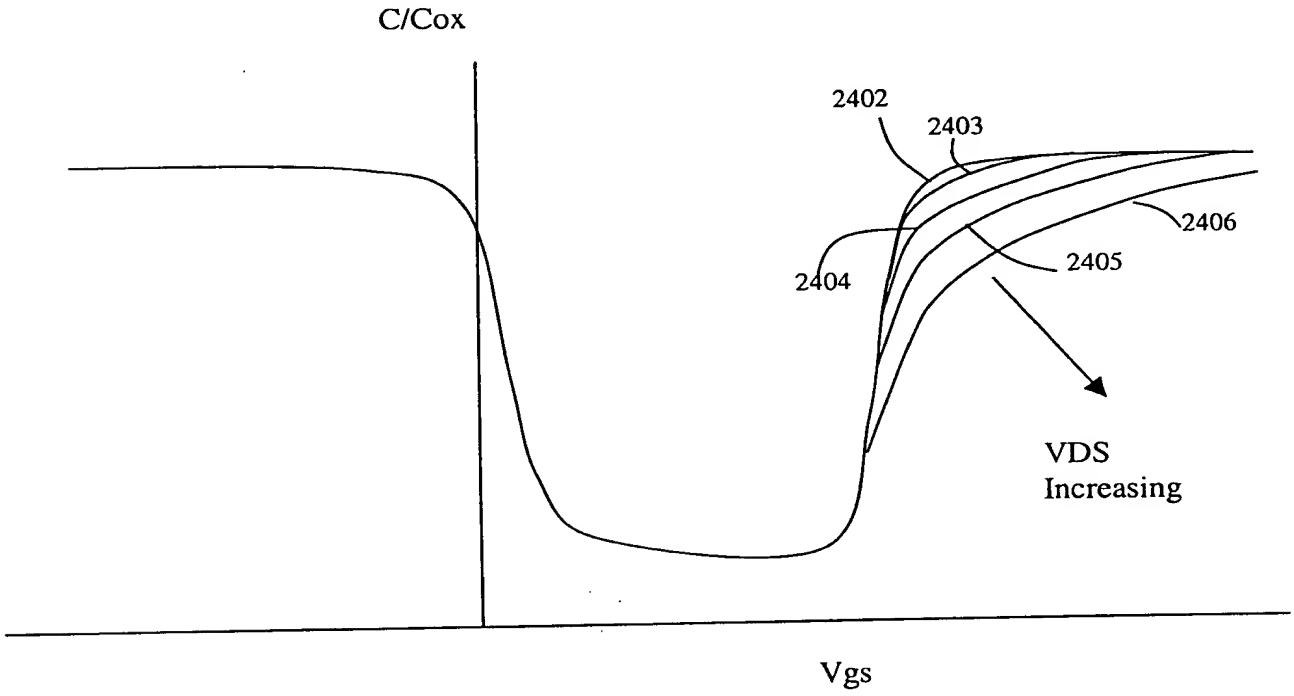


FIG. 25

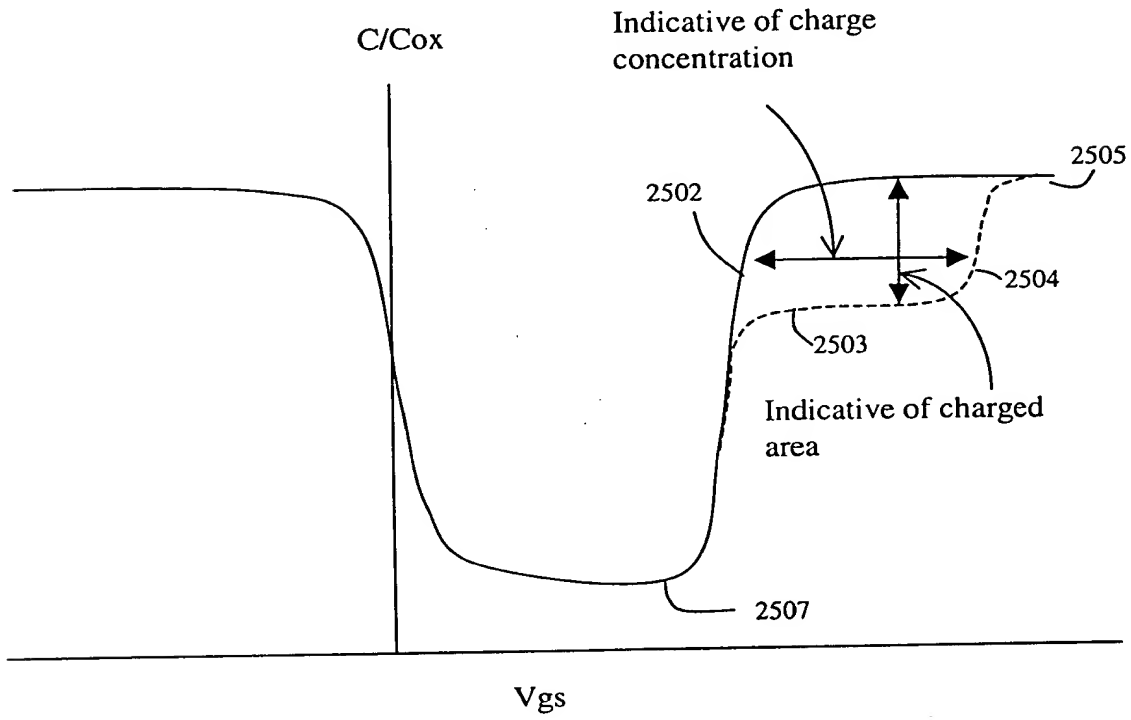

C/Cox
Indicative of charge concentration
2505
2502
2504
2503
Indicative of charged area
2507
Vgs

FIG. 26

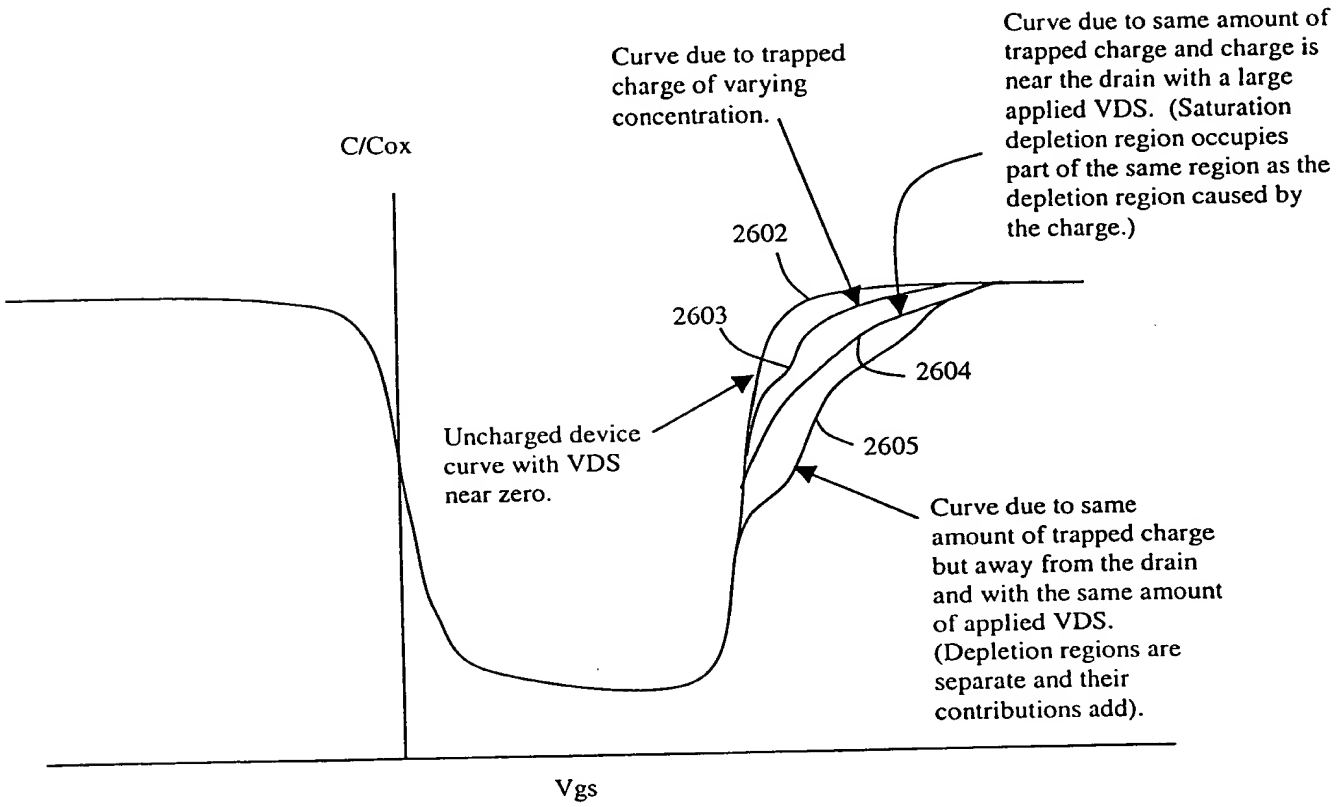

Curve due to trapped charge of varying concentration.
Curve due to same amount of trapped charge and charge is near the drain with a large applied VDS. (Saturation depletion region occupies part of the same region as the depletion region caused by the charge.)
C/Cox
2602
2603
2604
2605
Uncharged device curve with VDS near zero.
Curve due to same amount of trapped charge but away from the drain and with the same amount of applied VDS. (Depletion regions are separate and their contributions add).
Vgs

FIG.27

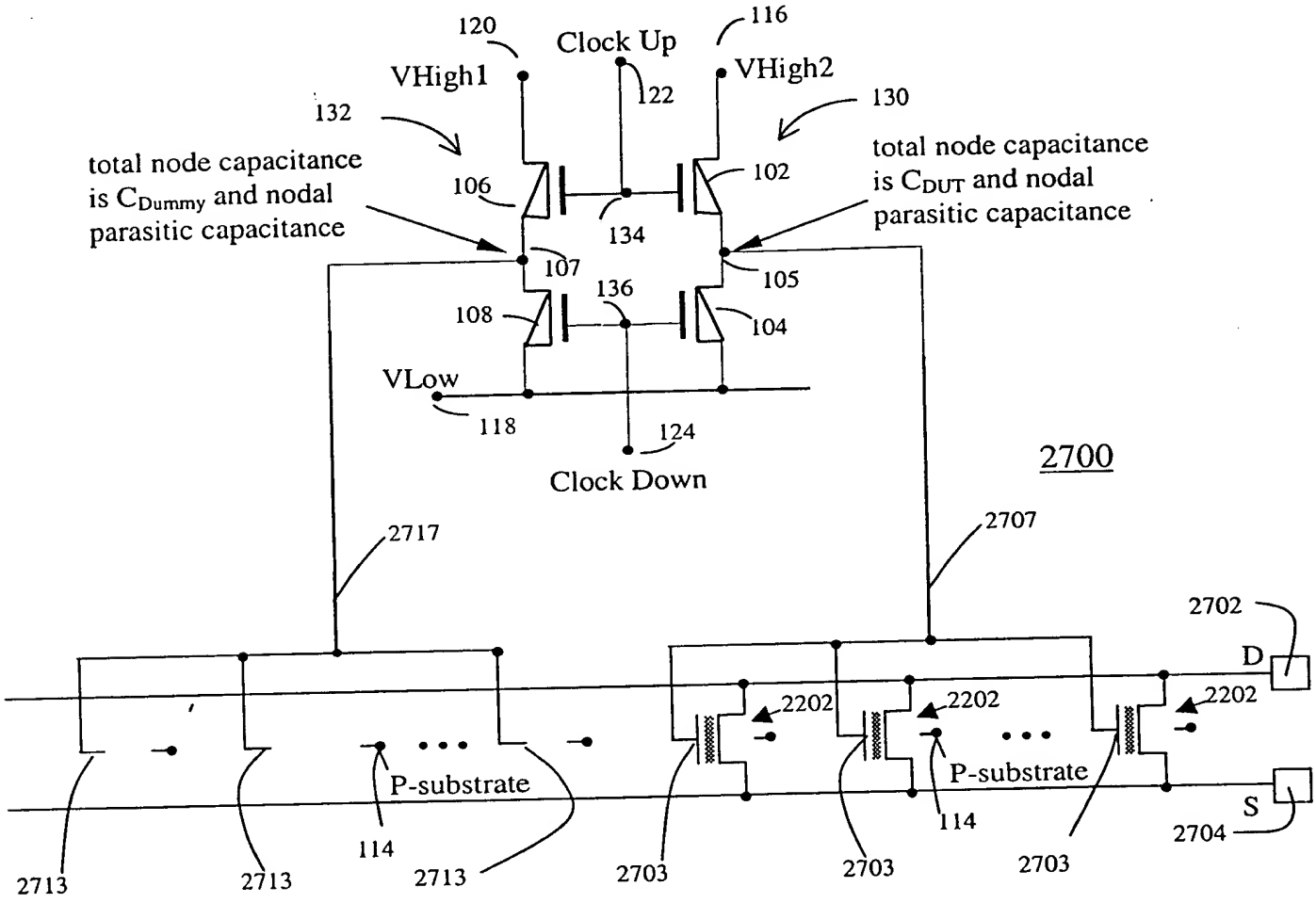

120
Clock Up
116
VHigh1
122
VHigh2
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
2700
2717
2707
2702
D
2202
2202
2202
P-substrate
P-substrate
114
114
S
2704
2713
2713
2713
2703
2703
2703

FIG.28

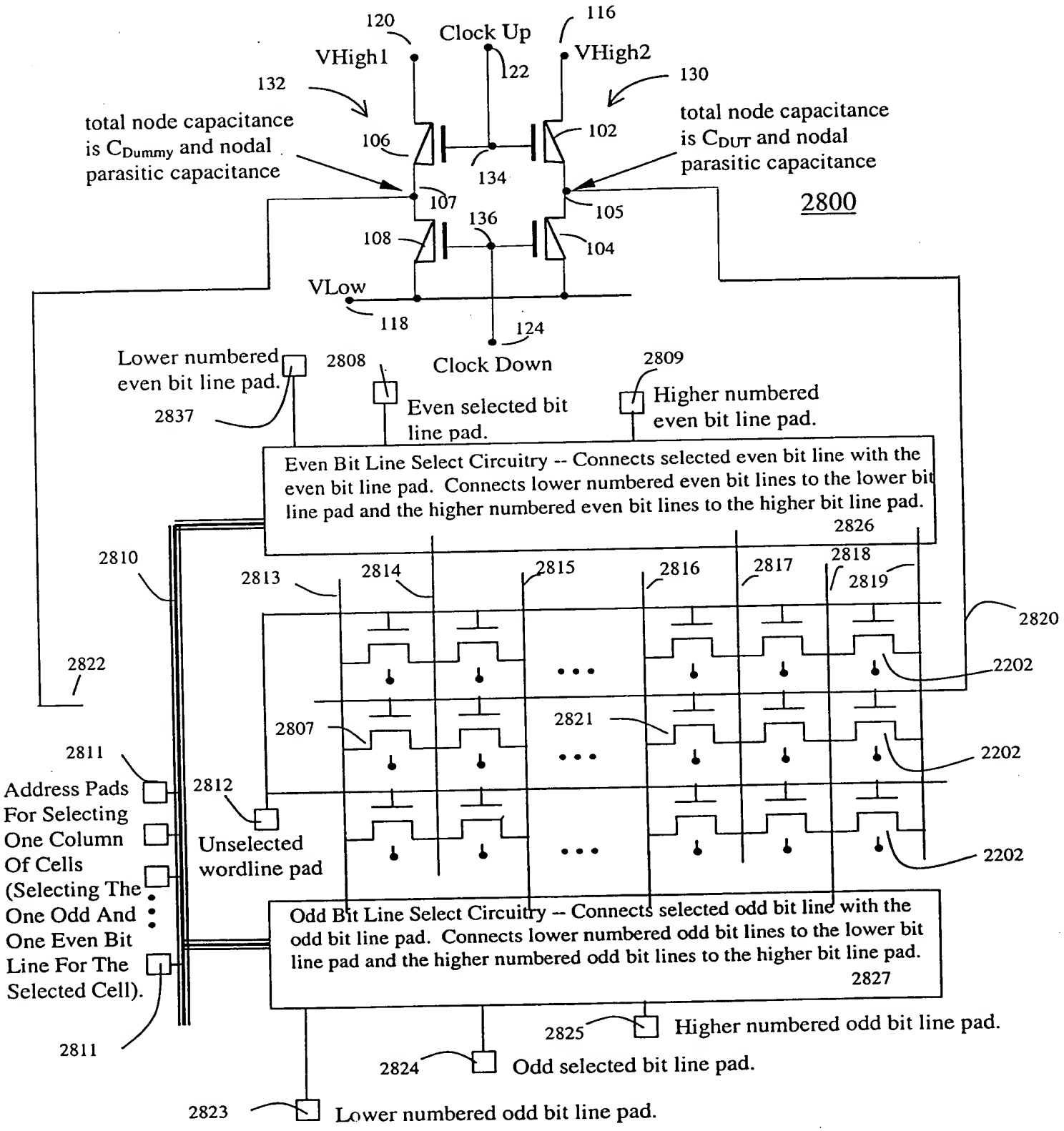

120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
2800
136
108
104
VLow
118
124
Clock Down
Lower numbered even bit line pad.
2808
2809
Even selected bit line pad.
Higher numbered even bit line pad.
2837
Even Bit Line Select Circuitry -- Connects selected even bit line with the even bit line pad. Connects lower numbered even bit lines to the lower bit line pad and the higher numbered even bit lines to the higher bit line pad.
2826
2810
2813
2814
2815
2816
2817
2818
2819
2820
2822
2202
2807
2821
2811
Address Pads For Selecting One Column Of Cells (Selecting The One Odd And One Even Bit Line For The Selected Cell).
2812
Unselected wordline pad
Odd Bit Line Select Circuitry -- Connects selected odd bit line with the odd bit line pad. Connects lower numbered odd bit lines to the lower bit line pad and the higher numbered odd bit lines to the higher bit line pad.
2827
2825
Higher numbered odd bit line pad.
2824
Odd selected bit line pad.
2823
Lower numbered odd bit line pad.

FIG.29

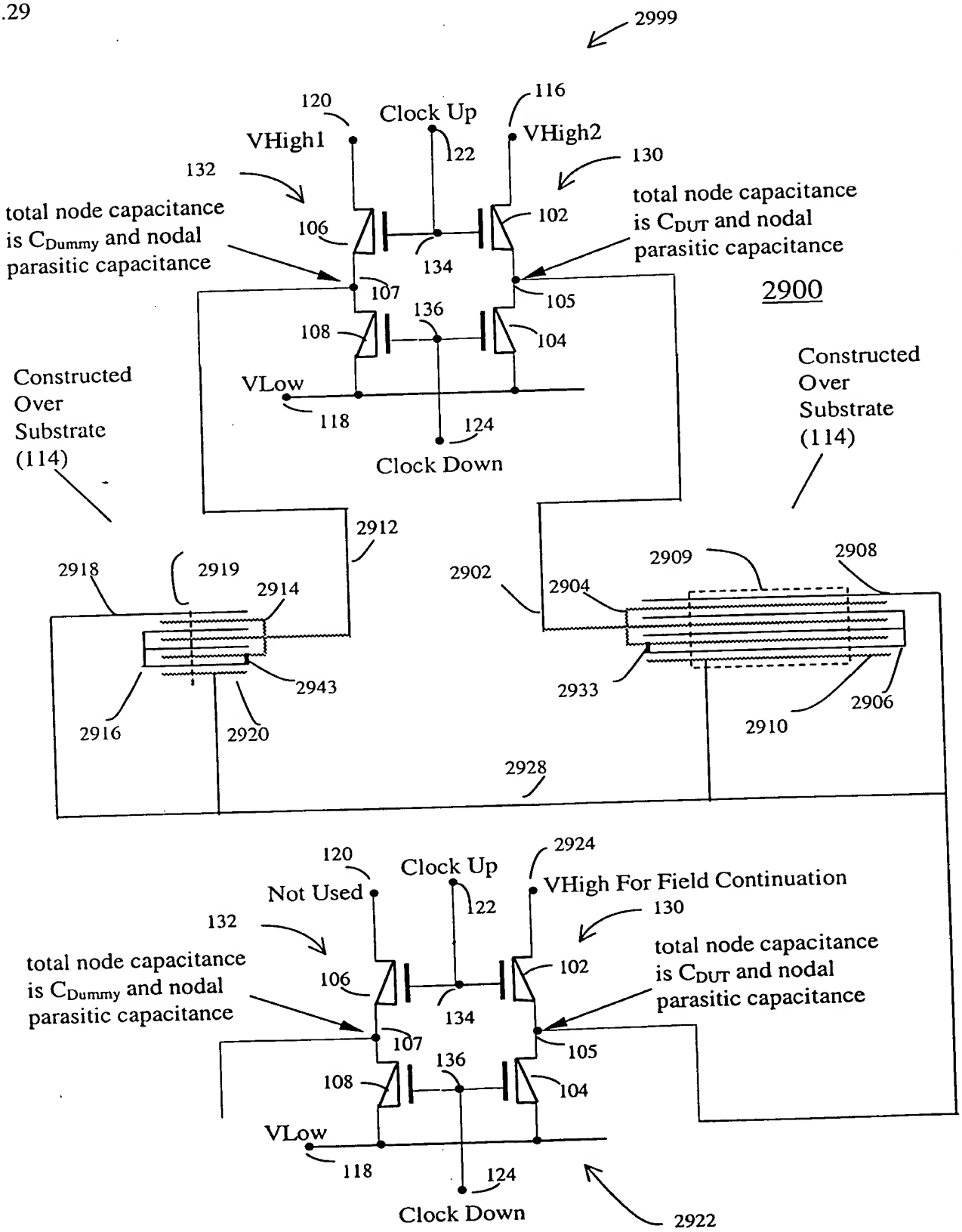

2999
120
Clock Up
116
VHigh1
VHigh2
122
130
132
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
2900
136
108
104
Constructed Over Substrate (114)
VLow
118
124
Clock Down
Constructed Over Substrate (114)
2912
2918
2919
2914
2902
2904
2909
2908
2943
2933
2906
2916
2920
2910
2928
120
Clock Up
2924
Not Used
VHigh For Field Continuation
122
130
132
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
2922

FIG.30

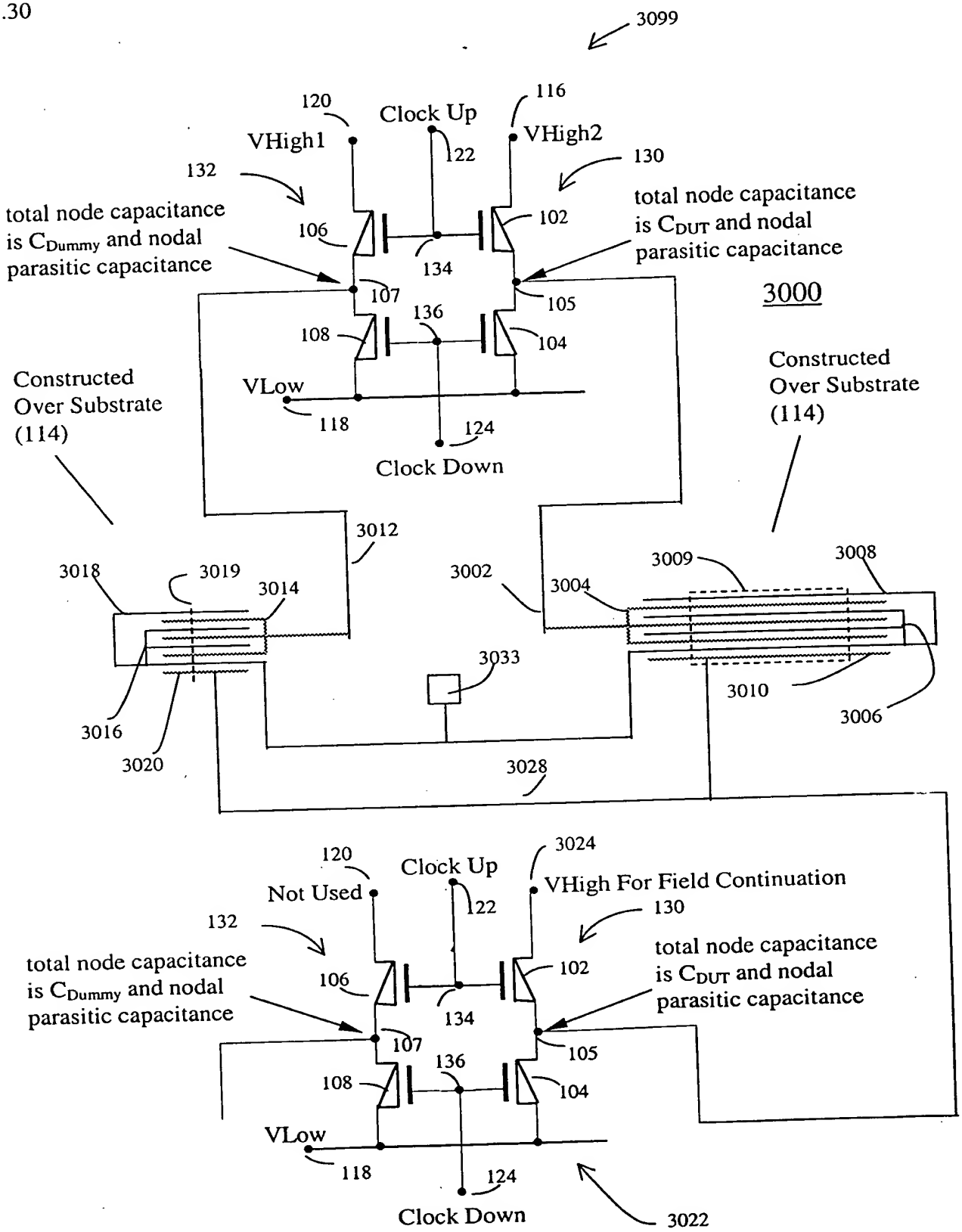

3099
120
Clock Up
116
VHigh1
VHigh2
122
130
132
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
3000
136
108
104
Constructed Over Substrate (114)
VLow
Constructed Over Substrate (114)
118
124
Clock Down
3012
3018
3019
3014
3002
3004
3009
3008
3033
3010
3016
3006
3020
3028
120
Clock Up
3024
Not Used
VHigh For Field Continuation
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
3022

FIG.31

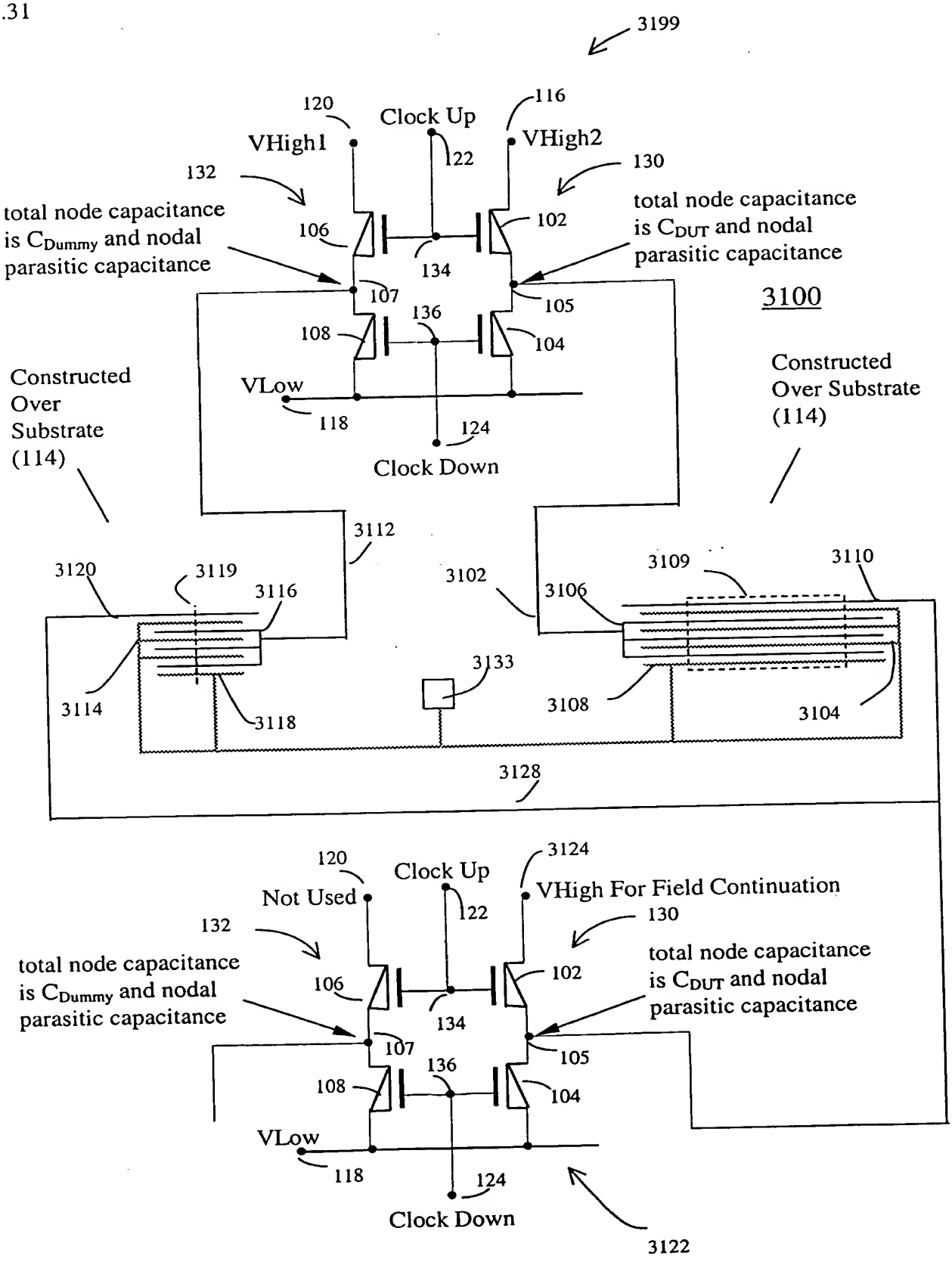

3199
120
Clock Up
116
VHigh1
VHigh2
22
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
3100
136
108
104
Constructed Over Substrate (114)
VLow
Constructed Over Substrate (114)
118
124
Clock Down
3112
3120
3119
3116
3102
3109
3110
3106
3133
3114
3118
3108
3104
3128
120
Clock Up
3124
Not Used
VHigh For Field Continuation
22
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
3122

FIG.32

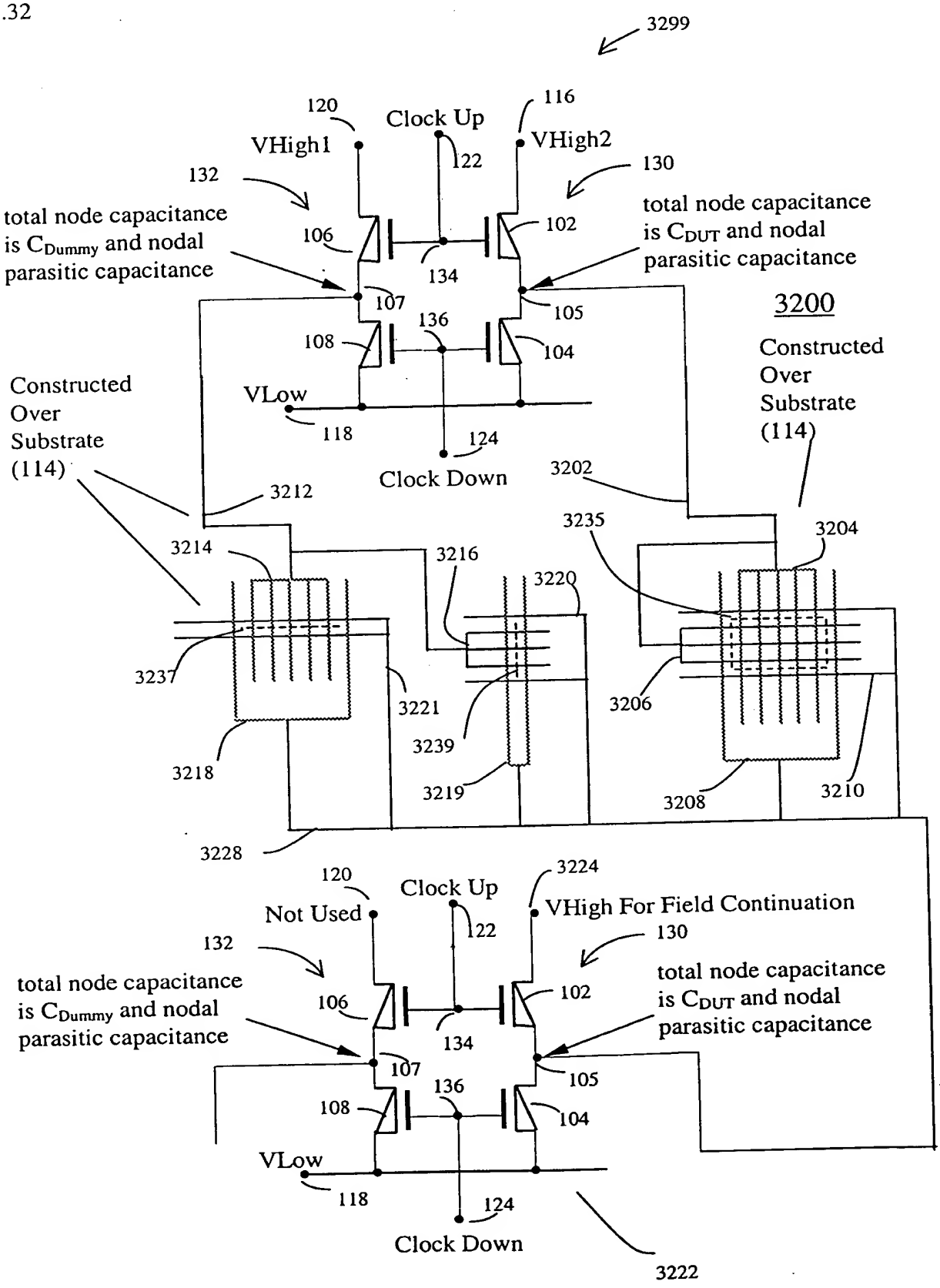

3299
120
Clock Up
116
VHigh1
VHigh2
122
130
132
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
3200
136
108
104
Constructed Over Substrate (114)
VLow
118
124
Clock Down
3202
3212
3235
3204
3214
3216
3220
3237
3221
3206
3239
3218
3219
3208
3210
3228
120
Clock Up
3224
Not Used
VHigh For Field Continuation
122
130
132
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
3222

FIG.33

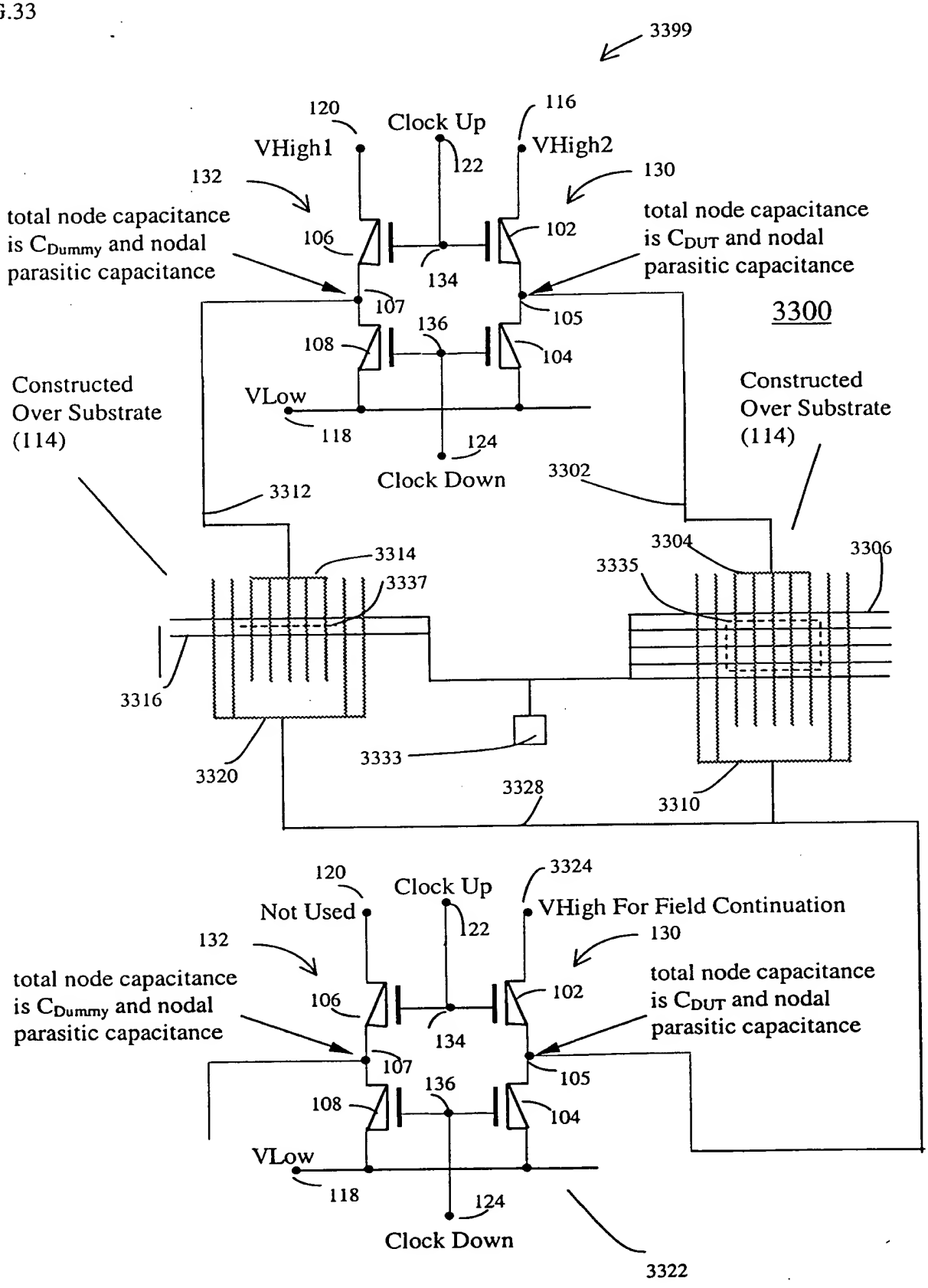

3399
120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
3300
136
108
104
Constructed Over Substrate (114)
VLow
Constructed Over Substrate (114)
118
124
Clock Down
3302
3312
3304
3306
3314
3335
3337
3316
3333
3320
3328
3310
120
Clock Up
3324
Not Used
VHigh For Field Continuation
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
3322

FIG.34

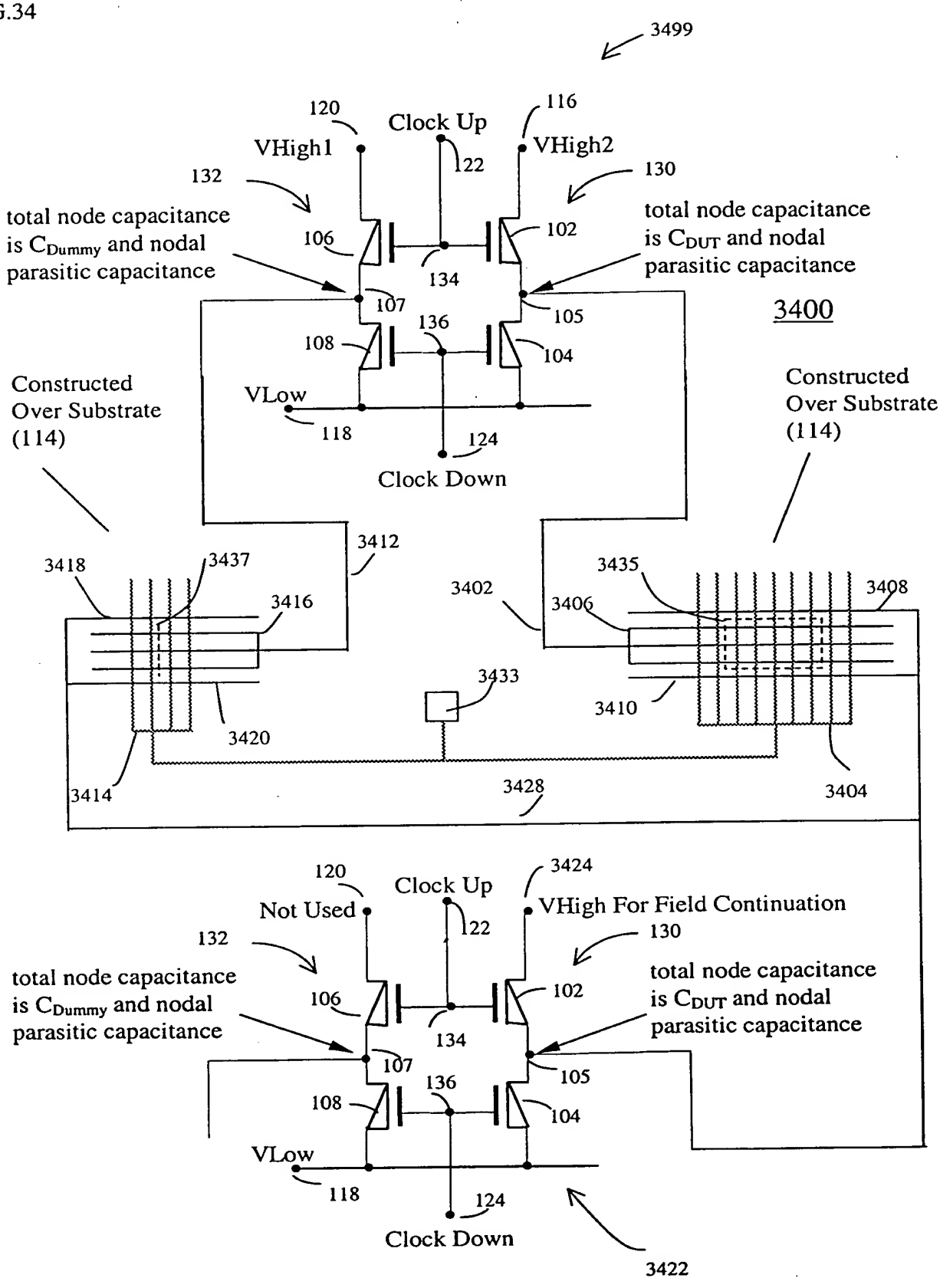
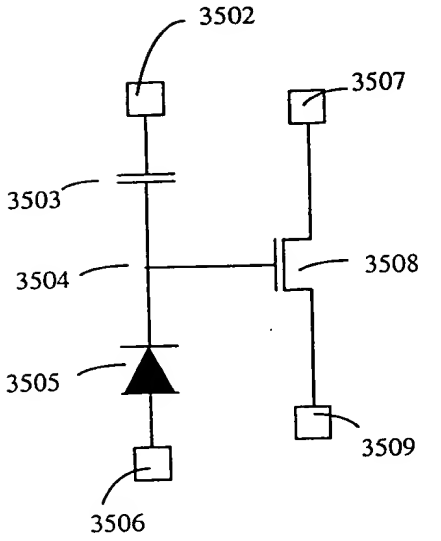

3499
120
Clock Up
116
VHigh1
VHigh2
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
3400
136
108
104
Constructed Over Substrate (114)
VLow
Constructed Over Substrate (114)
118
124
Clock Down
3412
3418
3437
3435
3408
3402
3406
3416
3433
3410
3420
3414
3428
3404
120
Clock Up
3424
Not Used
VHigh For Field Continuation
122
132
130
total node capacitance is C_{Dummy} and nodal parasitic capacitance
106
102
total node capacitance is C_{DUT} and nodal parasitic capacitance
134
107
105
136
108
104
VLow
118
124
Clock Down
3422

FIG. 35



3500

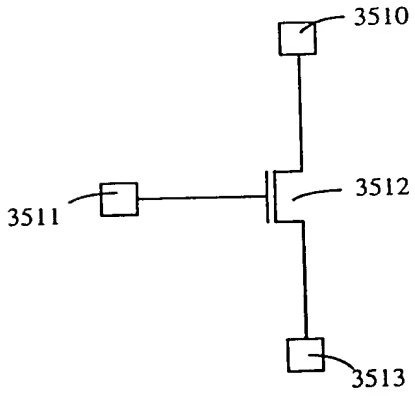
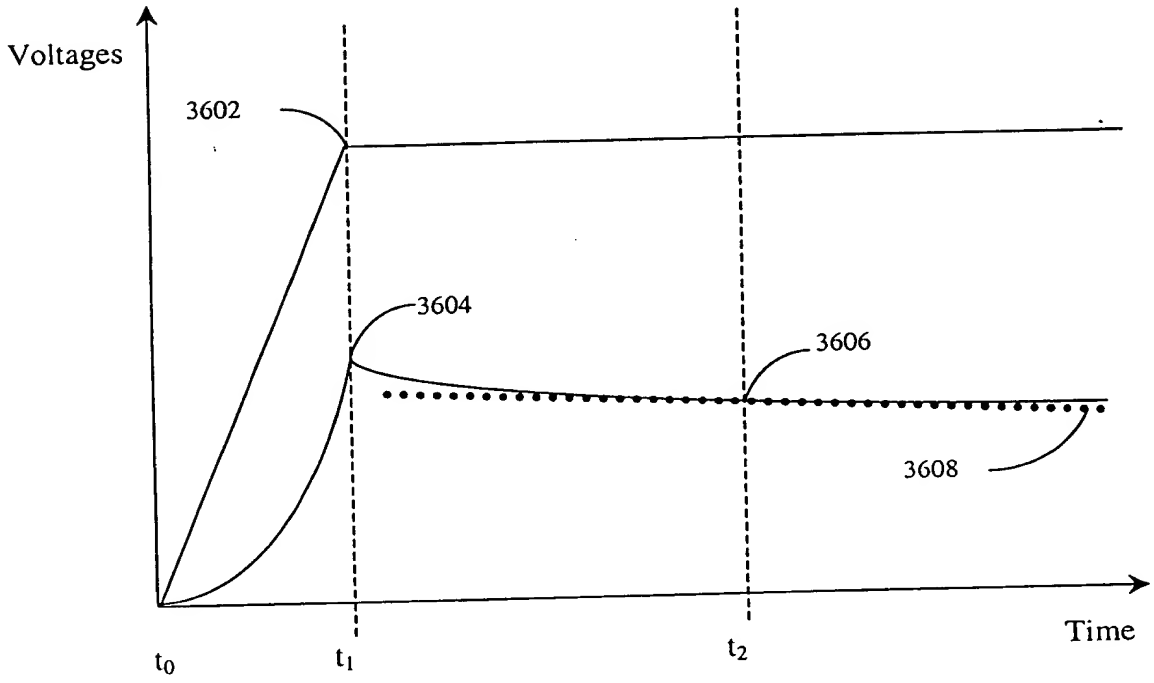
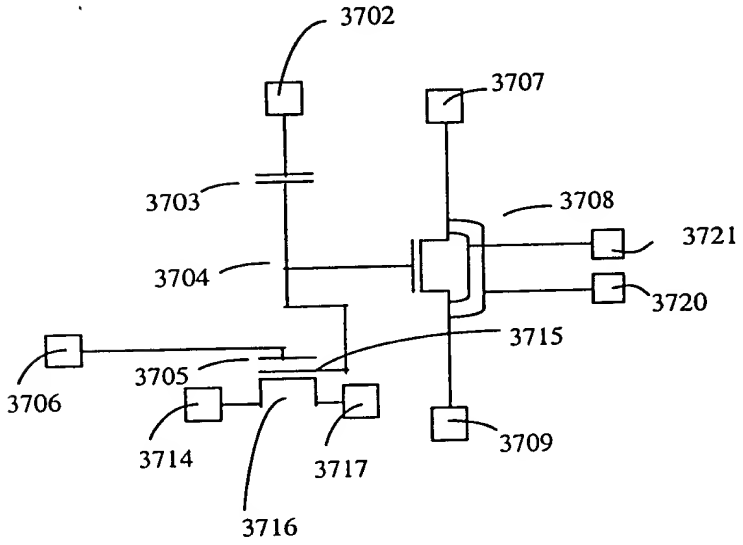


FIG. 36



3600

FIG. 37


3702
3707
3703
3708
3721
3704
3720
3715
3705
3706
3709
3714
3717
3716

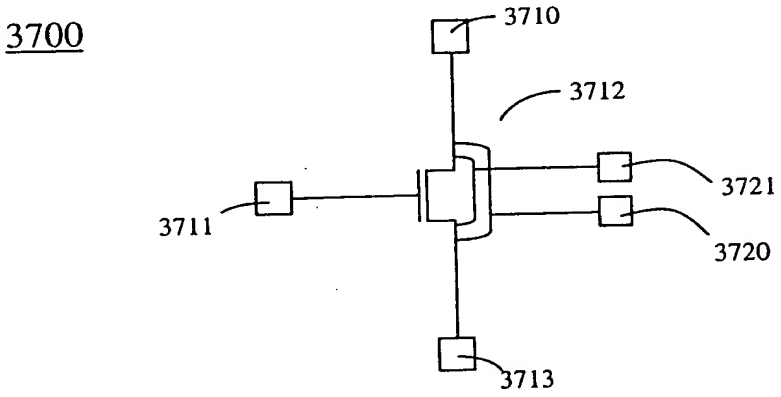
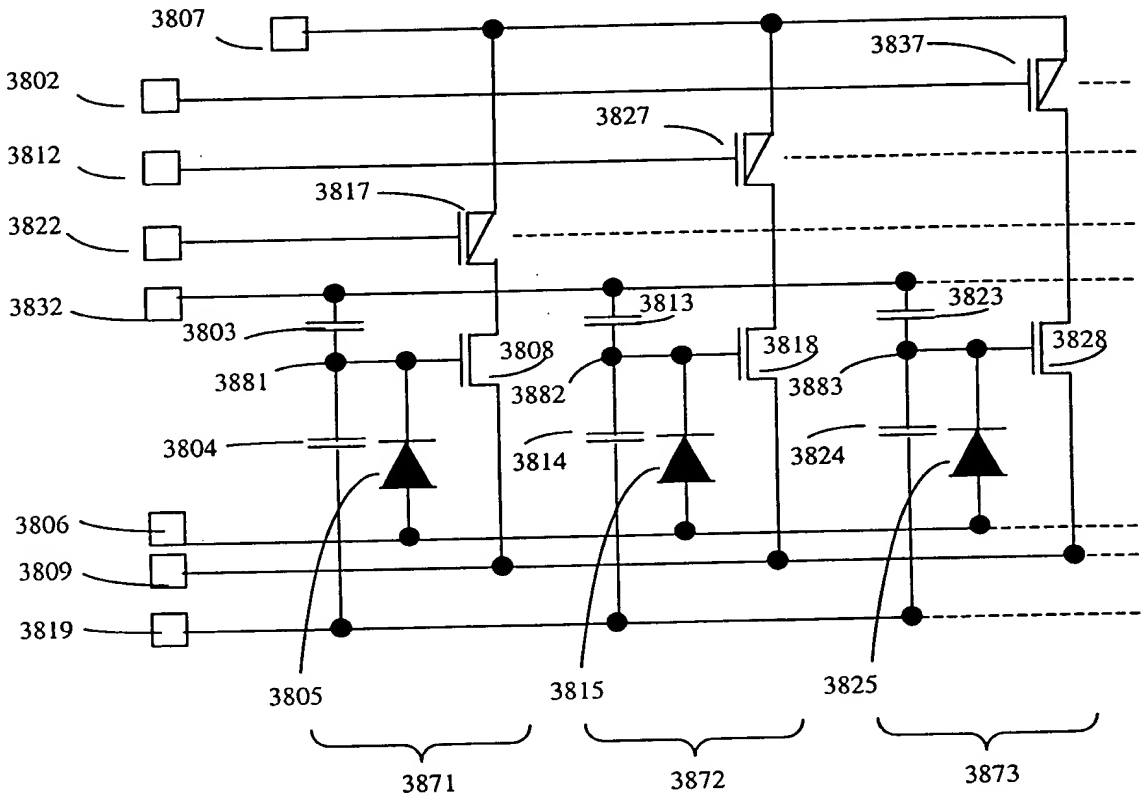
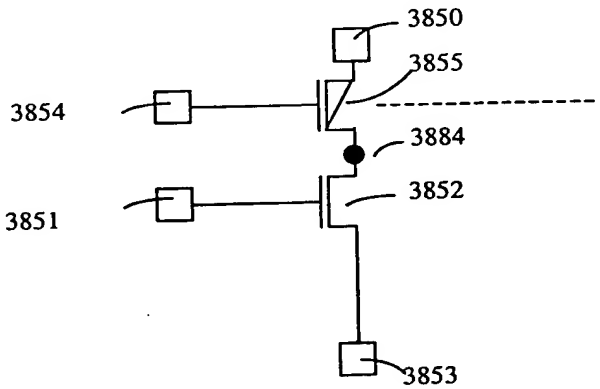

3700
3710
3712
3721
3711
3720
3713

FIG. 38


3807
3802
3812
3822
3832
3803
3881
3804
3806
3809
3819
3805
3817
3808
3827
3837
3813
3882
3814
3818
3883
3824
3823
3828
3815
3825
3871
3872
3873

3800


3850
3855
3854
3884
3852
3851
3853